COURSE OUTLINE

School/Faculty	Computing/Engineering	Page:	1 of 5
Programme Name	Bachelor of Computer Science (Network & Security)		
Course code:	SCSR 1013	Academic Session/Semester:	2018019/2
Course name:	DIGITAL LOGIC	Pre/co requisite:	NIL
Credit hours:	3		

Course synopsis	Digital electronics is the foundation of all microprocessor-based systems found in computers, robots, automobiles, and industrial control systems. This course introduces the students to digital electronics and provides a broad overview of many important concepts, components, and tools. Students will get up-to-date coverage of digital fundamentals-from basic concepts to programmable logic devices. Laboratory experiments provide hands-on experience with the simulator software, actual devices and circuits studied in the classroom			
Course coordinator	Marina Md Arshad			
Section	**Course Lecturers**	**Office**	**Telephone 07 55**	**E-mail @utm.my**
01	Dr Mohd Fo'ad Rohani	347-02	32374	foad
02 & 03	Marina Md Arshad	347-08	32369	marinama

Mapping of the Course Learning Outcomes (CLO) to the Programme Learning Outcomes (PLO), Teaching & Learning (T&L) methods and Assessment methods:

No.	CLO	PLO (ICGPA CODE)	Weight (%)	*Taxonomies and **generic skills	T&L methods	Assessment methods***
CLO1	Apply the fundamental of digital knowledge concept and basic and numbering systems to digital logic circuit.	KW	15	C3	Lecture Tutorial	T1
CLO2	Design combinational logic circuit using logic gates and Boolean algebra	KW	36	C4, P4	Lecture Tutorial, Lab	L1, L2, T2, F
CLO3	Design sequential asynchronous and synchronous circuits using fundamentals of latches and flip-flops.	KW	34	C4, P4	Lecture Tutorial Practical Lab	L3, F
CLO4	Effectively design and implement digital logic circuit based on practical problem.	AP, PS	15	C6, P5	Problem-based learning	GR, D
Refer *Taxonomies of Learning and **UTM's Graduate Attributes for measurement of outcomes achievement. ***T – Test; Q – Quiz; HW – Homework; L – Lab, GR – Group Report; PR – Personal Report; D - Demo, F – Final Exam etc.						

Details on Innovative T&L practices:

No.	Type	Implementation
1.	Active learning	Conducted through in-class activities
2.	Project-based learning	Conducted through design project. Students in a group of 2 design projects that require digital logic solutions involving the design and verification using real devices. Compliance to the design specifications need to be given in the form of written reports and demo.

Prepared by:	Certified by:
Name: Mohd Fo'ad Rohani (Course Owner) Signature: Date: 09 September 2017	Name: Professor Muhammad Shafie Abd Latiff (Director of Computer Science) Signature: Date:

Weekly Schedule:

WEEK 1 (15-19 Sept)	**Class briefing** **Module 1: Digital Logic Overview** Digital and Analogue Quantities, Binary Digits, Logic Levels and Digital Waveforms, Introduction to Logic Operations, Overview of Logic Functions, Fixed-Function IC, Programmable Logic Device (PLD)
WEEK 2 (22-26 Sept)	CHINESE NEW YEAR BREAK
WEEK 3 (29 Sept - 3 Oct)	**Module 2: Number Systems and Codes** Numbering System (Decimal, Binary, Octal and Hexadecimal), Number Conversion between Bases, Binary to Octal and Hexadecimal Conversion, Codes: BCD, GRAY, Parity, ASCII Arithmetic Operations: Integer (Unsigned, Signed Number) Operations: Addition and Subtraction
WEEK 4 (6 - 17 Octo)	**Module 3: Logic Gates (Lab 1)** Inverter (NOT), AND, OR, NAND, NOR, XOR and XNOR Gates Introduction to DEEDS
WEEK 5 (13 - 17 Octo)	**Module 4: Boolean Algebra and Logic Simplification** Laws and Rules of Boolean Algebra, DeMorgan's Theorem **Test 1: TUE 26 Feb 2019. 2-4pm. N28, BK6 & BK7**
WEEK 6 (20 - 24 Octo)	Combinational Logic Representation (Boolean to Logic Circuit, Logic Circuit to Boolean, Boolean to Truth Table, Logic Circuit to Truth Table), Simplification Using Boolean Algebra, Standard Forms of Boolean Expressions (SOP and POS Form), Karnaugh Map (K-Map), K-Map Minimisation (SOP and POS), Don't Care Conditions
WEEK 7 (27 - 31 Octo)	
WEEK 8 (3 - 7 Nov)	**Module 5: Combinational Logic Circuit (Lab 2)** Basic Combinational Logic Circuits (AND-OR, AND-OR-INVERT, XOR, XNOR), Universal Property of NAND and NOR, Dual Symbol, Design a Combinational Circuit **27 – 28 MAR: MID SEMESTER BREAK**
WEEK 9 (10 - 14 Nov)	
WEEK 10 (17 - 21 Nov)	**Module 6: Functions of Combinational Logic** Basic and Parallel Binary Adders, Comparators, Decoders, Encoders, Multiplexer (Data Selector), Demultiplexer, Code Converter, Parity Generator/ Checker
WEEK 11 (24 - 28 Nov)	**Module 7: Latches, Flip-Flops and Timers** Latch (SR, Gated SR and Gated D), Flip-flop (SR, JK, D, T) **Test 2: TUE 9 April 2019. 2-4pm. N28, BK6 & BK7**
WEEK 12 (1 - 5 Dec)	**Module 8: Counters (Lab 3) (Project 1 - Report) (Project 2 – Demo)** Types of Sequential Circuits, Counters, Design and Analysis of Asynchronous Counter, Operation (Up/Down, Truncated), Asynchronous Counter Decoder, Flip-flop Excitation Table, Design and Analysis of Synchronous Counter (Up/Down, Truncated), Counter for Arbitrary Sequences, Cascaded Counter, Analysis of Sequential Circuits (SR, JK, D, T)
WEEK 13 (8 - 12 Dec)	
WEEK 14 (15 - 19 Dec)	
WEEK 15 (22 - 26 Dec)	**Module 9: Shift Register** Basic Shift Register Functions, SISO, SIPO, PISO, PIPO, Bidirectional Shift Register, Shift Register Counter (Ring and Johnson Counter)

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Transferable skills (generic skills learned in course of study which can be useful and utilised in other settings):

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Student learning time (SLT) details:

Distribution of course content	Teaching and Learning Activities						TOTAL SLT
	Guided Learning (Face to Face)				Guided Learning Non-Face to Face	Independent Learning Non-Face to face	
CLO	**L**	**T**	**P**	**O**			
CLO 1	8	1				7.5	**16.5H**
CLO 2	11	4	1			25.2	**41.2H**
CLO 3	8	2	0.5			22.8	**33.3H**
CLO4	4		2			10	**16H**
Total SLT	**31**	7	3.5			**65.5**	**107h**

Continuous Assessment		PLO	Percentage	Total SLT
1	Lab 1 (CLO2)	KW	3	**1.5H**
2	Lab 2 (CLO2)	KW	3	**1.5H**
3	Lab 3 (CLO3)	KW	3	**1.5H**
4	Project 1 (Report) (CLO4)	AP	8	**1H**
5	Project 2 (Demo) (CLO4)	PS	8	**1H**
6	Test 1 (CLO1)	KW	15	**1.5H**
7	Test 2 (CLO2)	KW	25	**2H**
Final Assessment			Percentage	Total SLT
1	Final Exam (CLO2)	KW	5	**0.6h**
2	Final Exam (CLO3)	KW	30	**2.4h**
Grand Total SLT				**120h**

Special requirement to deliver the course (e.g: software, nursery, computer lab, simulation room):

Digital Logic Lab and Lab Assistant (TA) Software: Deeds Software, WinCUPL software, Wellon software, Universal Programmer Hardware: Burner device, ETS5000, Integrated Circuits (IC), IC Tester, Coloured wire.

Learning resources:

Text book (if applicable) Digital Logic (2018), School of Computing, Faculty of Engineering, UTMJB Digital Logic Lab Manual (2018), School of Computing, Faculty of Engineering, UTMJB

COURSE OUTLINE

Main references

Floyd, T.L., (2014), "Digital Fundamentals", 10th Edition, Prentice Hall, USA.

Additional references

Tocci, R.J., Widmer, N.S. and Moss, G.L, (2014), "Digital Systems", 11th Edition, Prentice Hall, USA.

Roth, C., (2014), "Fundamental of Logic Design", 7th Edition, Thomson Brooks, USA.

Online

http://elearning.utm.my

Academic honesty and plagiarism:

Assignments are individual tasks and NOT group activities (UNLESS EXPLICITLY INDICATED AS GROUP ACTIVITIES). Copying of work (texts, lab results etc.) from other students/groups or from other sources is not allowed. Brief quotations are allowed and then only if indicated as such. Existing texts should be reformulated with your own words used to explain what you have read. It is not acceptable to retype existing texts and just acknowledge the source as a reference. Be warned: students who submit copied work will obtain a mark of **zero** for the assignment and exams and disciplinary steps may be taken by the Faculty. It is also unacceptable to do somebody else's work, to lend your work to them or to make your work available to them to copy.

Other additional information (Course policy, any specific instruction etc.):

1. Attendance is compulsory and will be taken in every lecture session. Student with less than 80% of total attendance is not allowed to sit for final exam.
2. Students are required to behave and follow the University's dressing regulation and etiquette all the time.
3. Exercises and tutorial will be given in class and some may be taken for assessment. Students who do not do the exercise will lose the coursework marks for the exercise.
4. Assignments must be submitted on the due dates. Some points will be deducted for late submissions. Assignments submitted three days after the due date will not be accepted.
5. Make up exam will not be given, except to students who are sick and submit medical certificate confirmed by UTM panel doctors. Make up exam can only be given within one week of the initial date of exam.

		KW			AP	PS	
No.	**Assessment**	**CLO1**	**CLO2**	**CLO3**	**CLO4**	**CLO4**	**Total %**
1	**LAB 1**		3				**3**
2	**LAB 2**		4				**4**
3	**LAB 3**			3			**3**
4	**PROJECT 1 (REPORT)**				8		**8**
5	**PROJECT 2 (DEMO)**					7	**7**
6	**TEST 1**	15					**15**
7	**TEST 2**		25				**25**
8	**FINAL EXAM**		5	30			**35**
Total		15	36	34	8	7	**100**
		85			**8**	**7**	

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