4.1.2 Digital-to-Stochastic Converter (DSC)

4.1.2.1 Linear Feedback Shift Register (LFSR)

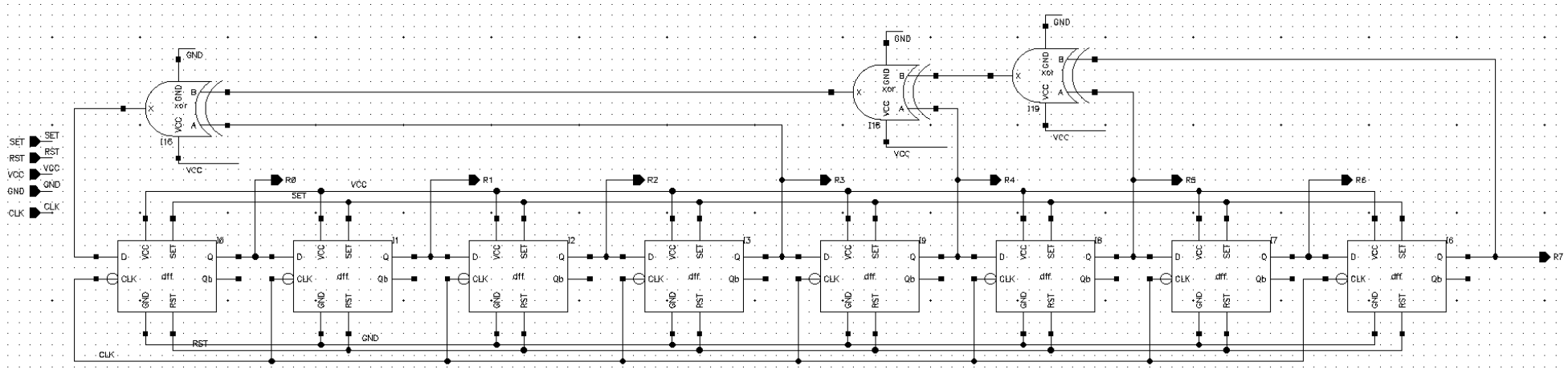

Figure 4.35: LFSR Schematic

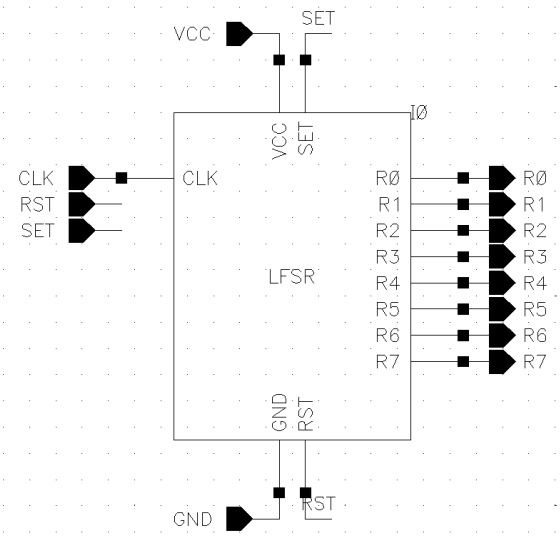

Figure 4.36: LFSR Symbol

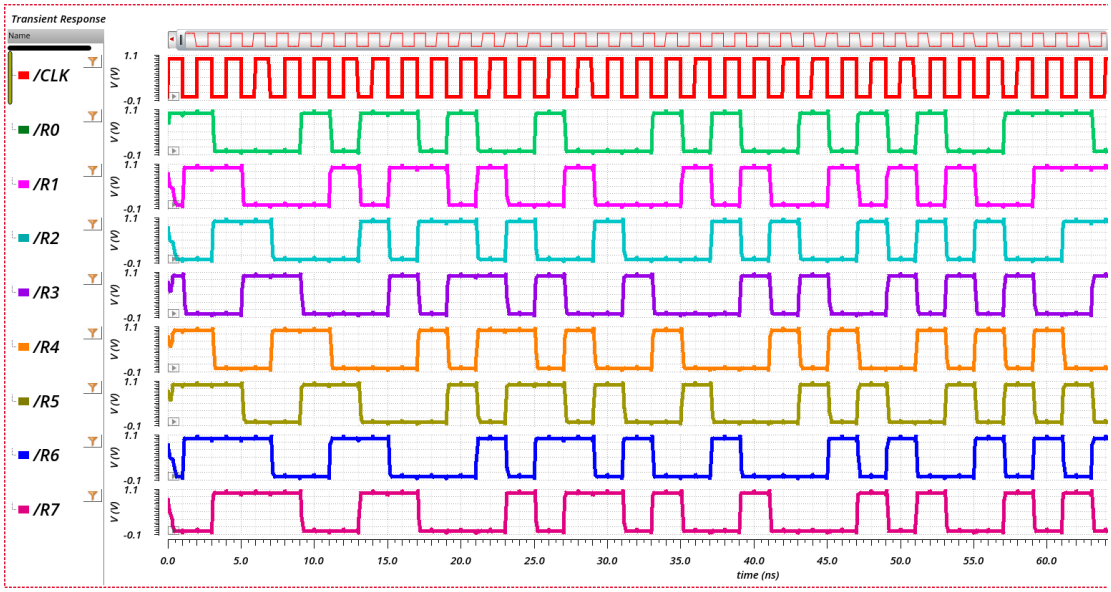

Figure 4.37: LFSR Waveform

Figure 4.35 shows the schematic of LFSR and Figure 4.36 shows its symbol. The symbol then goes through a testbench to determine its functionality. Figure 4.37 shows the LFSR Waveform output. This waveform shows that the LFSR successfully gave random output for each 8 bits. The data input to the LFSR is generated by XOR-ing the tap bits while the remaining bits function as a standard shift register. This LFSR is designed using the polynomial $X^8 + X^6 + X^5 + X^4 + 1$. Since the polynomial has the largest power of 8, thus the total random number sequences that will be generated by this LFSR is 2^8 -1 which is equal to 255 sequences.

4.1.2.2 Parallel-in Parallel Output (PIPO) Input Register

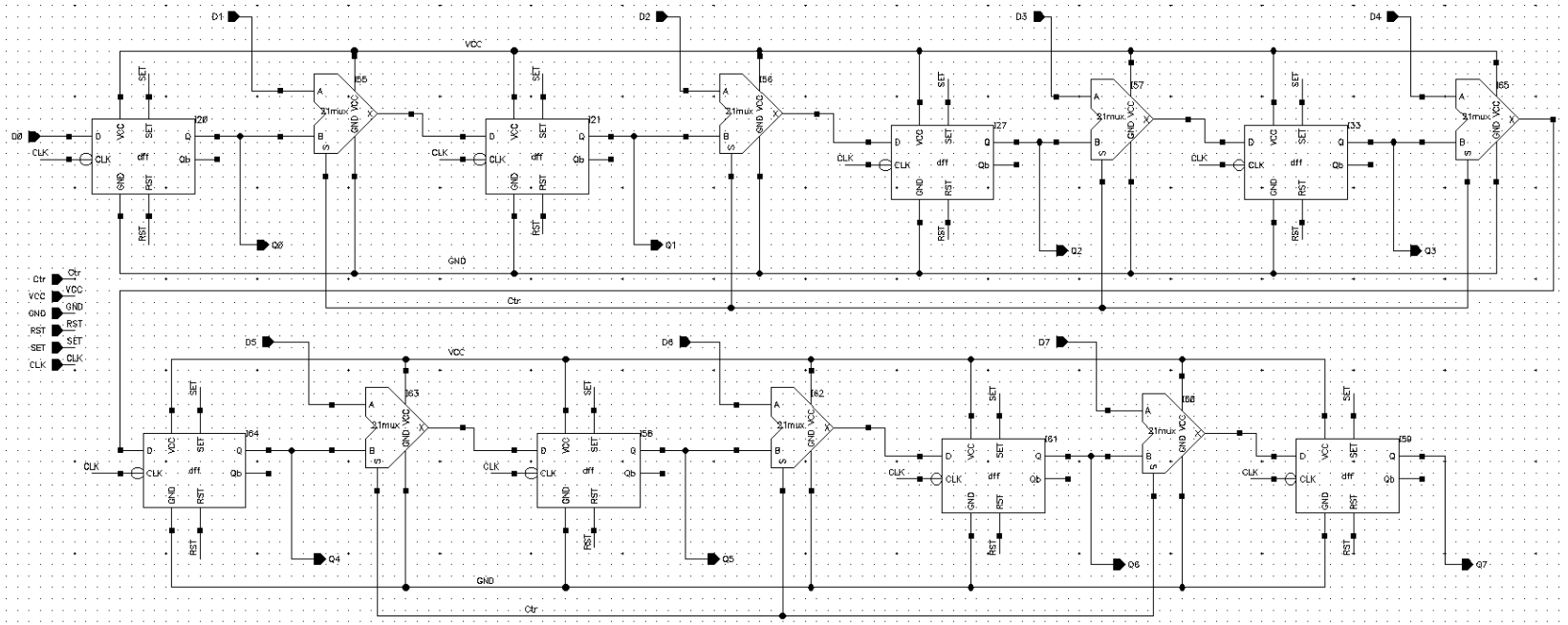

Figure 4.38: PIPO Schematic

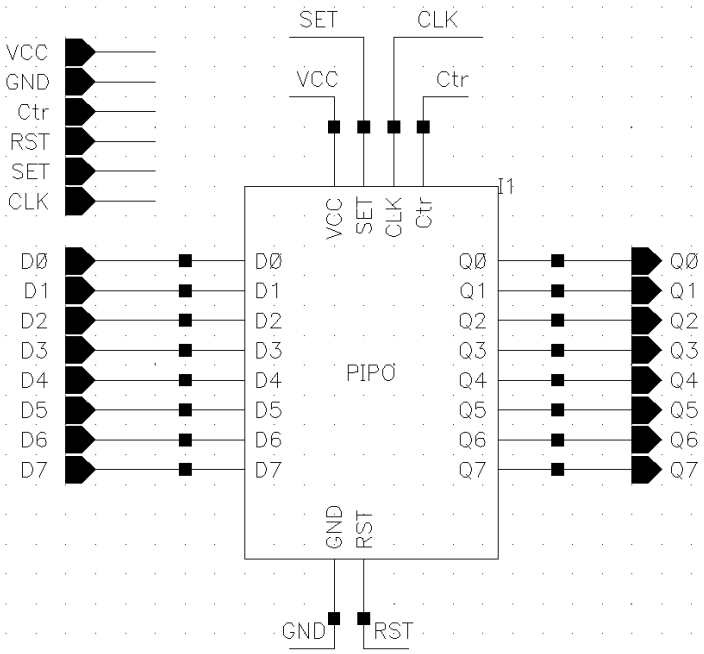

Figure 4.39: PIPO Symbol

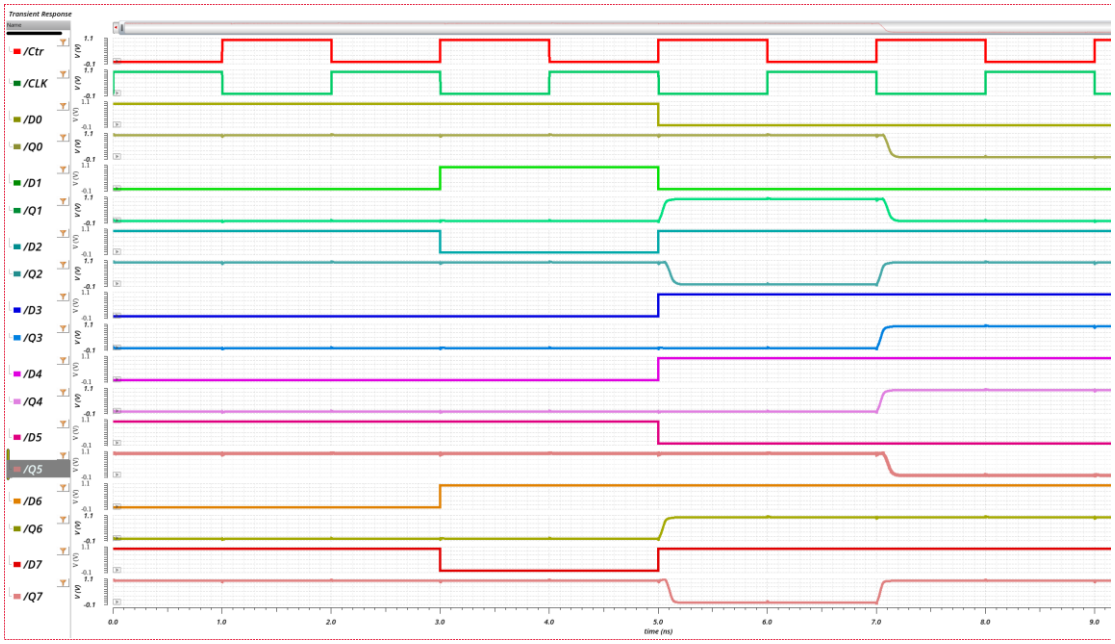

Figure 4.40: PIPO Waveform

Figure 4.38 shows the schematic of the PIPO input register and Figure 4.39 shows its symbol. The symbol then goes through a testbench to determine its functionality. Figure 4.40 shows the PIPO Waveform output. This waveform shows that the PIPO successfully load the parallel inputs simultaneously and transfers the value to their respective outputs on the next clock cycle.

4.1.2.3 Multi-Level Probability Conversion Circuit (MLPCC)

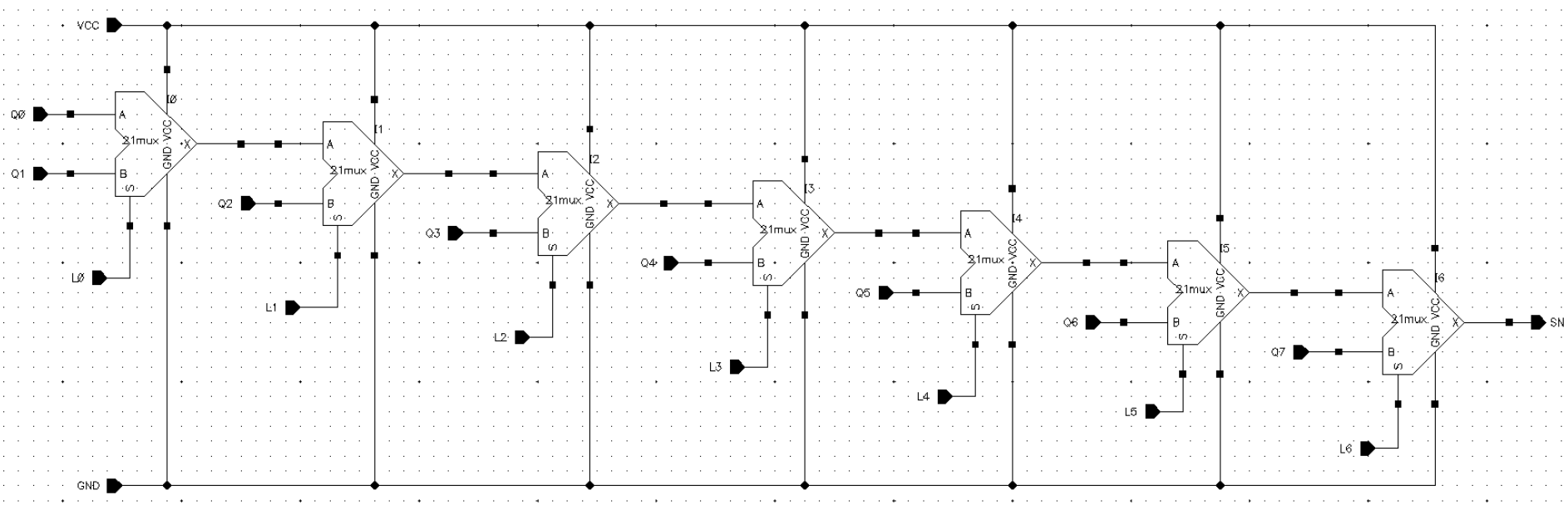

Figure 4.41: MLPCC Schematic

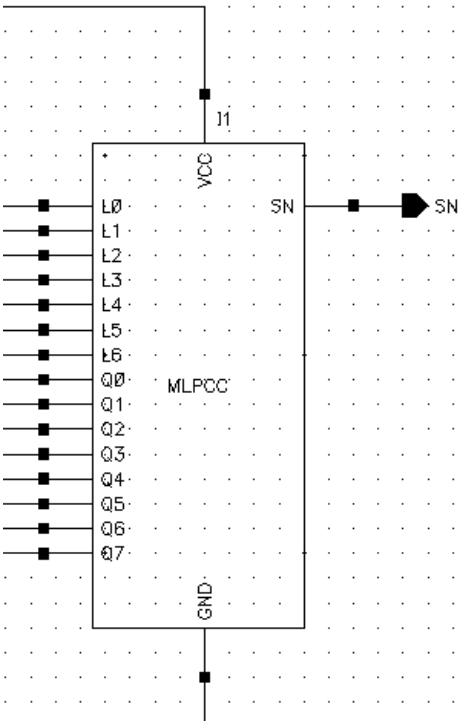

Figure 4.42: MLPCC Symbol

Figure 4.41 shows the schematic of MLPCC and Figure 4.42 shows its symbol. The simulation for MLPCC is conducted in the DSC Block due to the inputs are the outputs of both LFSR and PIPO.

4.1.2.4 Digital-to-Stochastic (DSC) Block

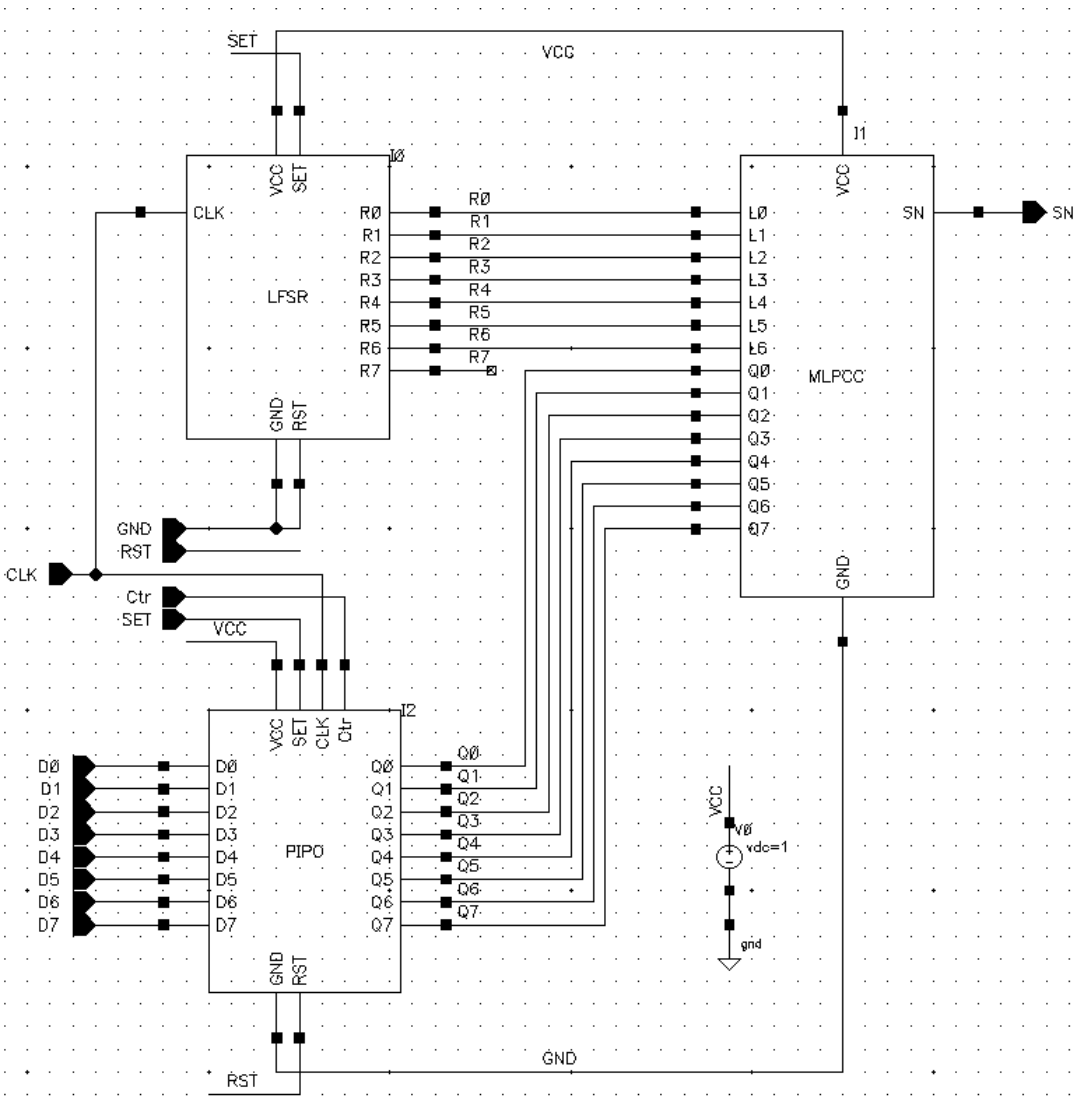

Figure 4.43: DSC Block Schematic

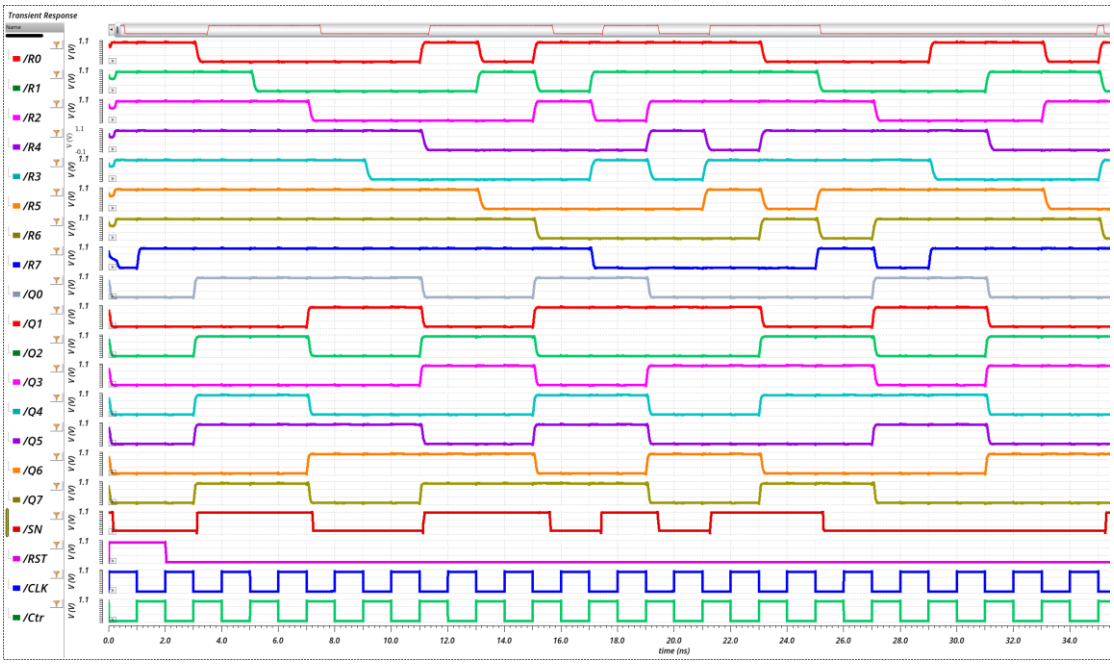

Figure 4.44: DSC Block Waveform

Figure 4.45: DSC Block Power Consumption

This DSC Block is the result of the combination of LFSR, PIPO, and MLPCC as shown in Figure 4.43. This DSC Block then goes through a testbench to determine its functionality. Figure 4.44 shows the Analog DSC Waveform output. This waveform shows that the DSC Block successfully produced a series output that is the Stochastic Number (Output SN). This happened because of the MLPCC managed to accept the inputs from LFSR (Input R0 to R7) and PIPO (Input Q0 to Q7), did a comparison with both inputs, and then generated a Stochastic output. However, since the output is in bitstream format, it's hard to determine the correlation between the Stochastic output with parallel inputs thus the MLPCC needs to be adjusted by adding an output pin for every output of the 2:1 multiplexer in order for us to be able to calculate the correlation. For power consumption, it is calculated that DSC block only used 18.77 µW during the simulation as shown in Figure 4.45.