4.1.3 Analog-to-Digital Converter (ADC)

4.1.3.1 Successive Approximation Register (SAR)

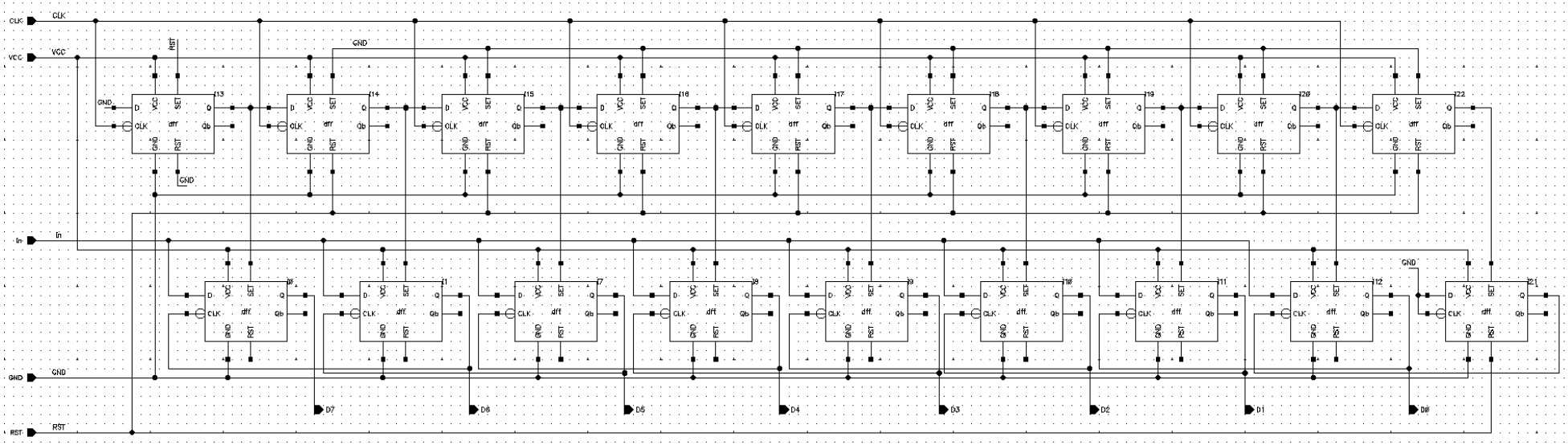

Figure 4.46: SAR Schematic

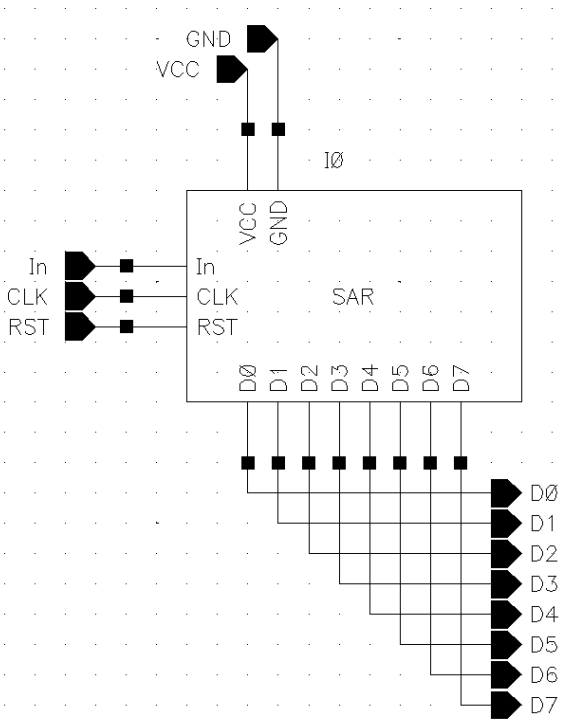

Figure 4.47: SAR Symbol

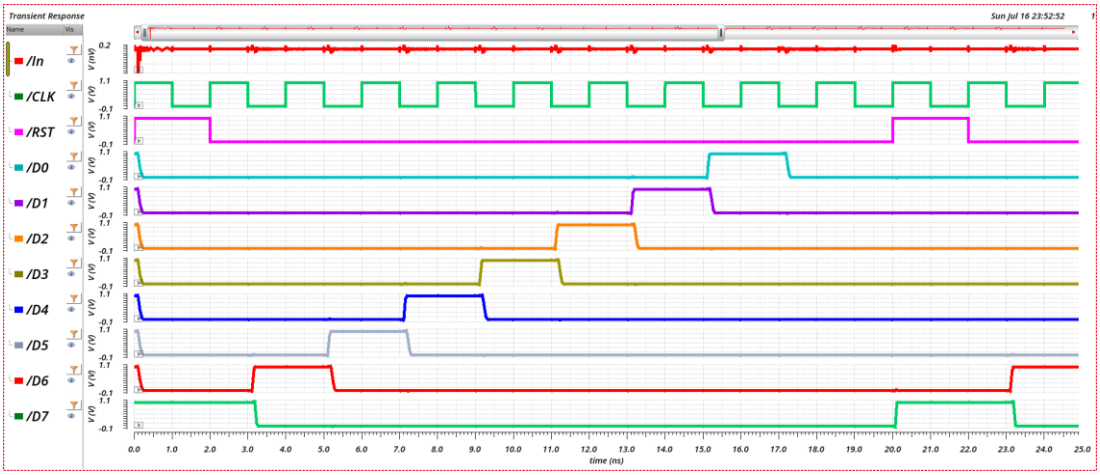

Figure 4.48: SAR Waveform

Figure 4.46 shows the schematic of SAR and Figure 4.47 shows its symbol. The symbol then goes through a testbench to determine its functionality. Figure 4.48 shows the SAR Waveform output. This waveform shows that the SAR is able to shift bit 1 when the comparator output is 0 and the first digital input of the DFF is 0. The outcome of the SAR is following the shifting bit 1 as shown in paper [64]. However, the SAR could not hold any value of the input, thus the SAR need to be adjusted with an addition of multiplexer to the DFF as shown in Figure 4.49 [64].

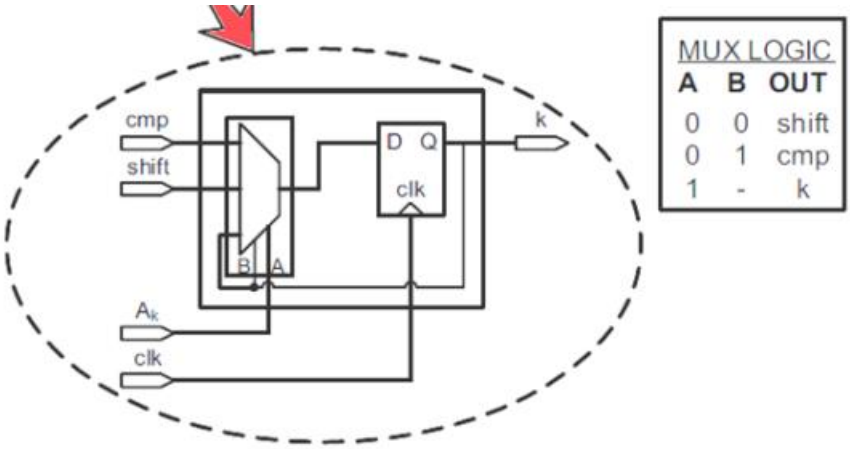

Figure 4.49: CMOS DFF with Mux

4.1.3.2 R-2R Ladder Digital-to-Analog Converter (DAC)

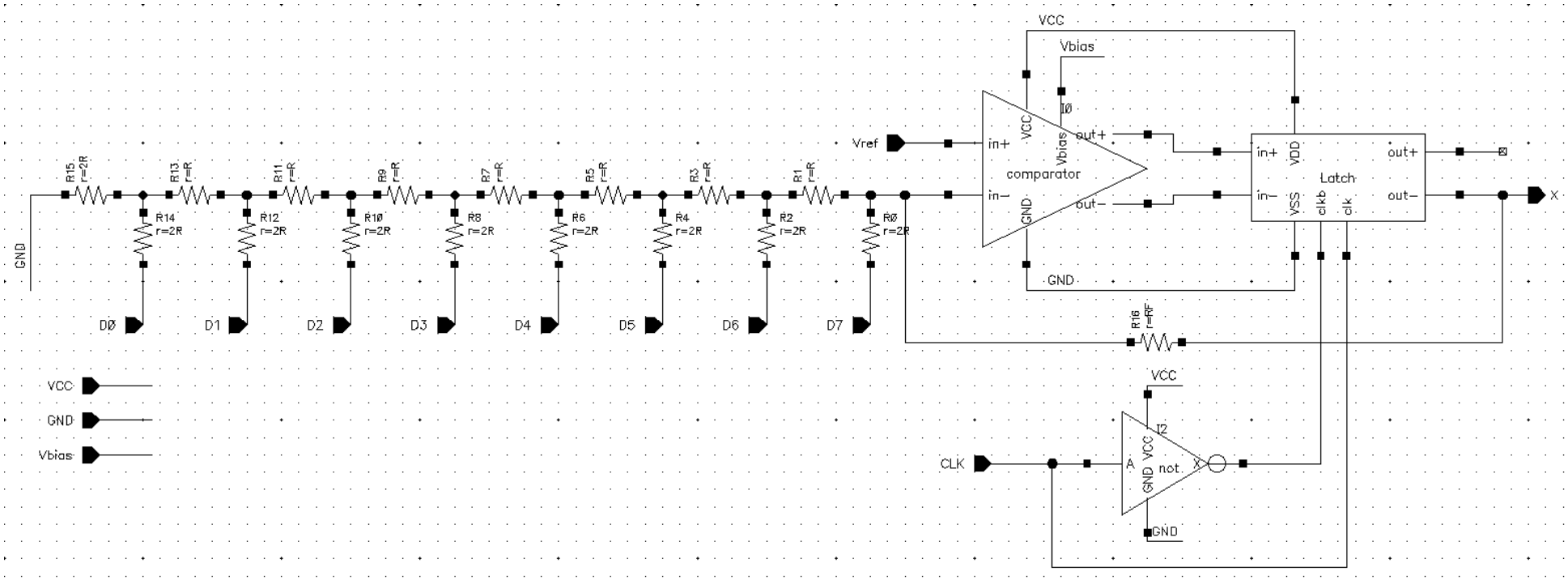

Figure 4.50: R-2R Ladder DAC Schematic

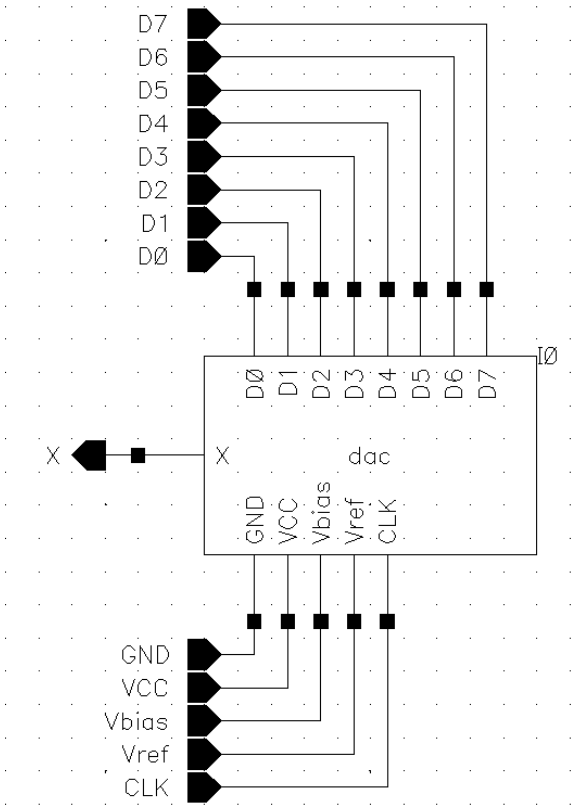

Figure 4.51: R-2R Ladder DAC Symbol

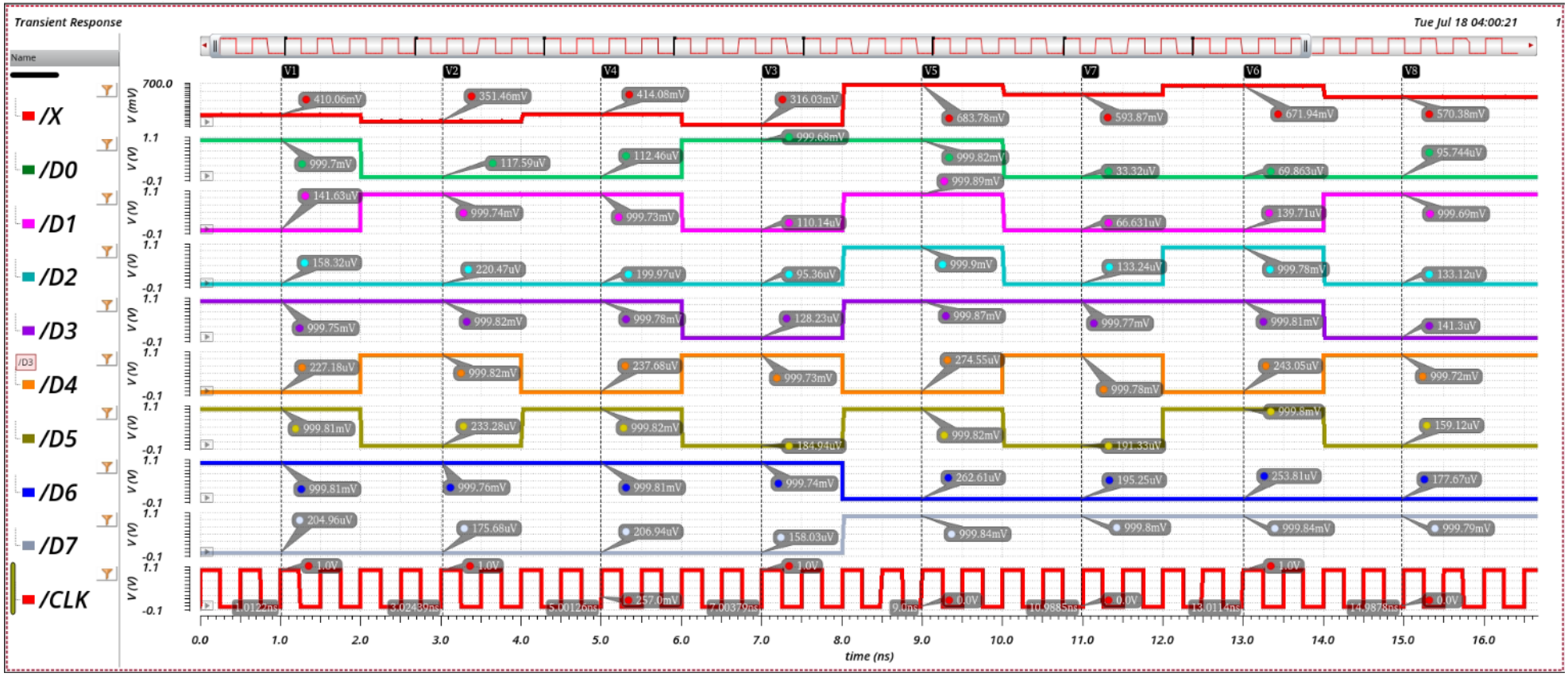

Figure 4.52: R-2R Ladder DAC Waveform

Figure 4.50 shows the schematic of R-2R Ladder DAC and Figure 4.51 shows its symbol. The symbol then goes through a testbench to determine its functionality. Figure 4.52 shows the R-2R Ladder DAC Waveform output. This waveform shows that the R-2R Ladder DAC is able to generate an analog output equivalent to its digital input counterpart. This is shown that the digital bitstreams of 01101001 (the first sequence) are able to produce an analog output of 0.410V which is the roughly the same with the calculation of 0.412V with only a margin error of 0.5%. This result value can be proven using the Voltage Output DAC formula in Equation 2. For all other sequences, the DAC shows that it can accurately convert every digital input into its analog output equivalent.

4.1.3.3 Internal Clock Generator (ICG)

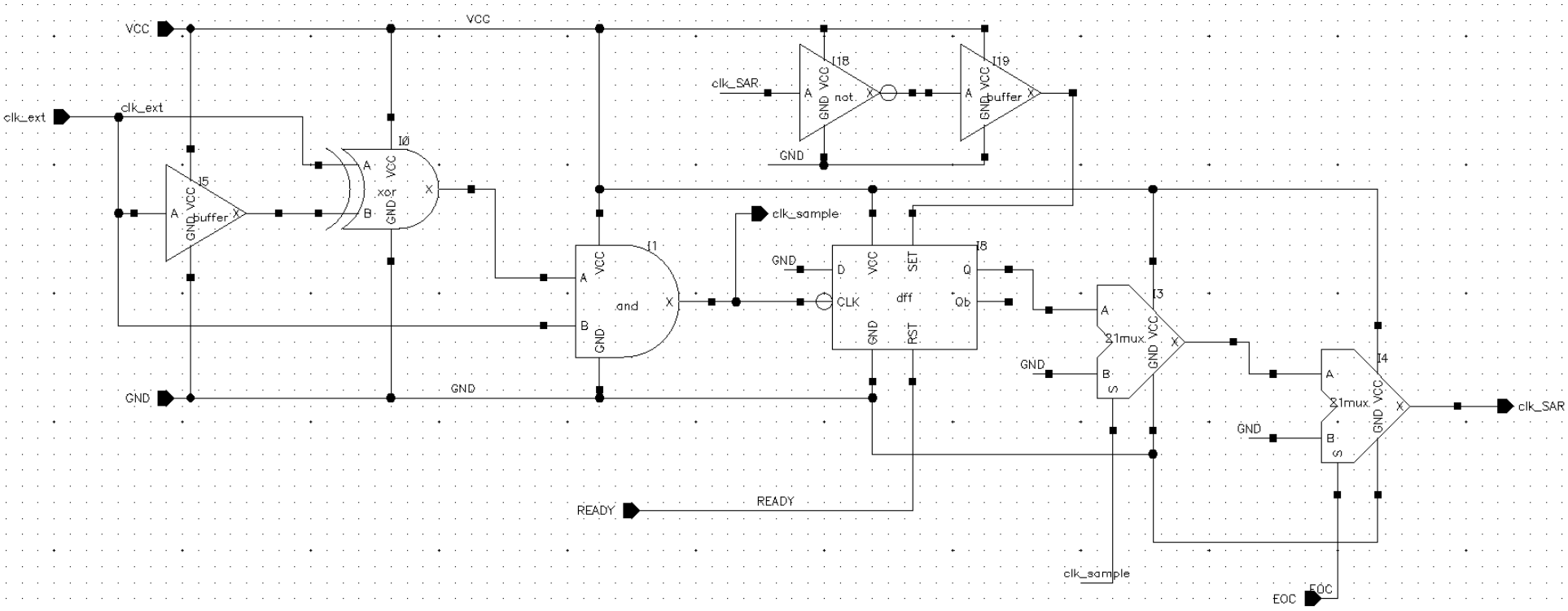

Figure 4.53: ICG Schematic

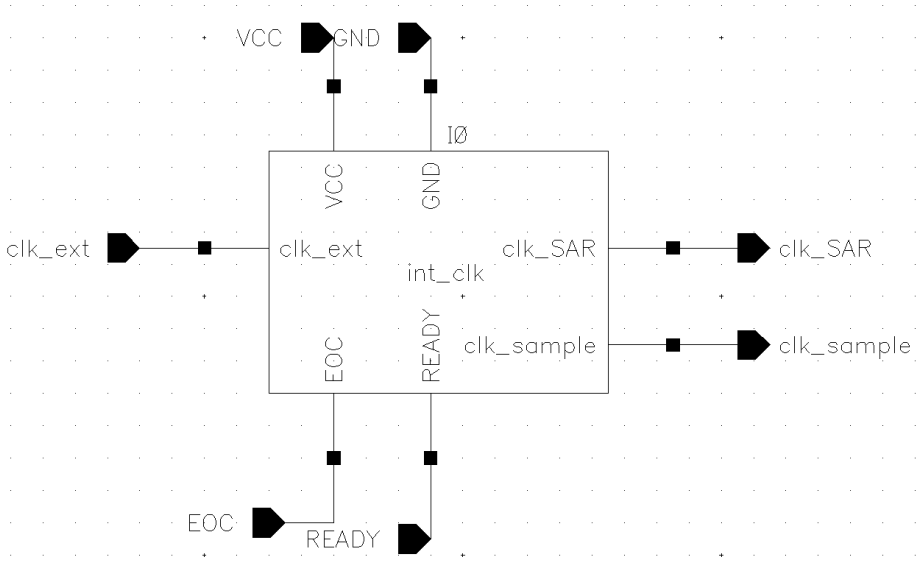

Figure 4.54: ICG Symbol

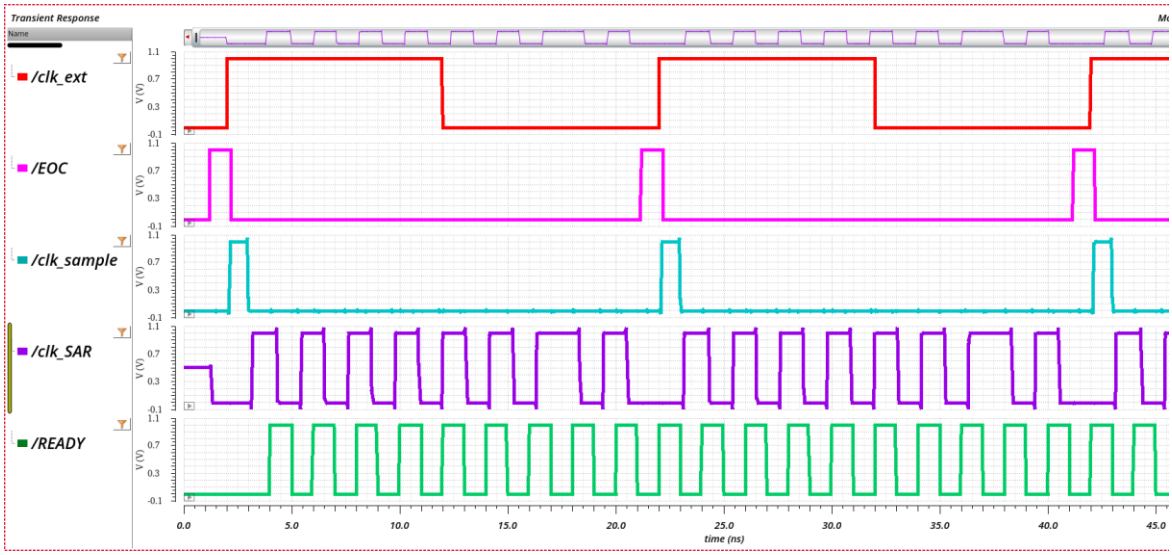

Figure 4.55: ICG Waveform

Figure 4.53 shows the schematic of ICG and Figure 4.54 shows its symbol. The symbol then goes through a testbench to determine its functionality. Figure 4.55 shows the ICG Waveform output. This waveform shows that the ICG successfully mimics the behavior of the ICG as shown in Figure 2.20. However, the clk_sar has a duty cycle exceeding 50% (on the 7th cycle), possibly due to the READY input. This situation will cause the SAR to have not enough time to run the whole process of SAR for that particular cycle. Thus, further research, try-and-error attempts, and adjustment with the ICG are needed in order to make sure that the ICG is able to properly function as intended.