

CHAPTER 4

PROPOSED WORK

4.1 Introduction

This chapter is focused on presenting the work progress of this project for each component and block based on the proposed planning in Chapter 3.

4.1.1 Standard Cells

4.1.1.1 NOT Gate

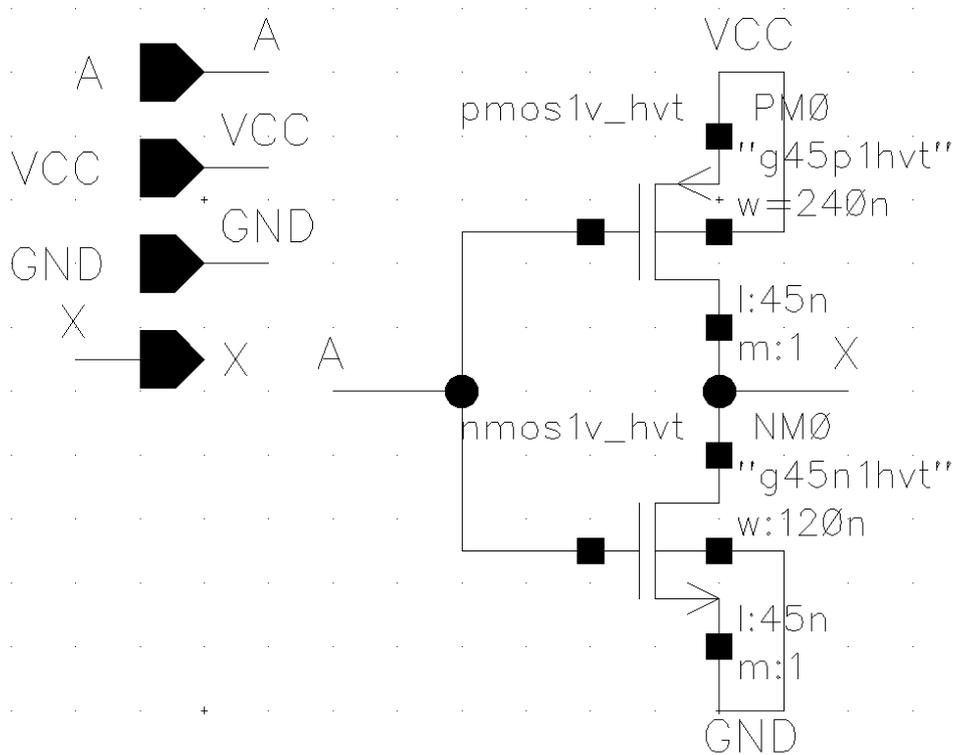


Figure 4.1: NOT Gate Schematic

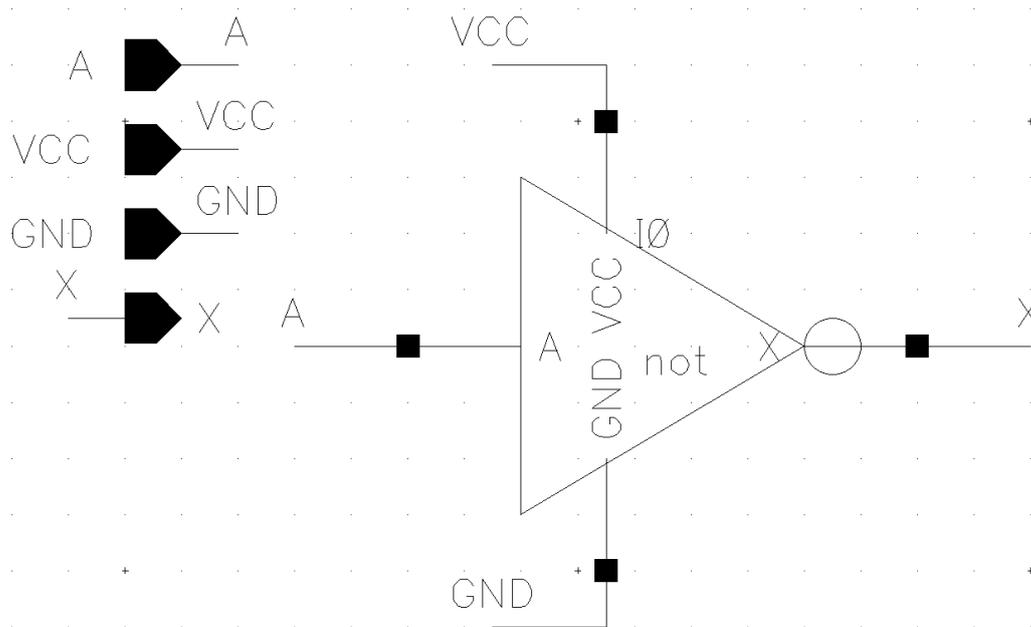


Figure 4.2: NOT Gate Symbol

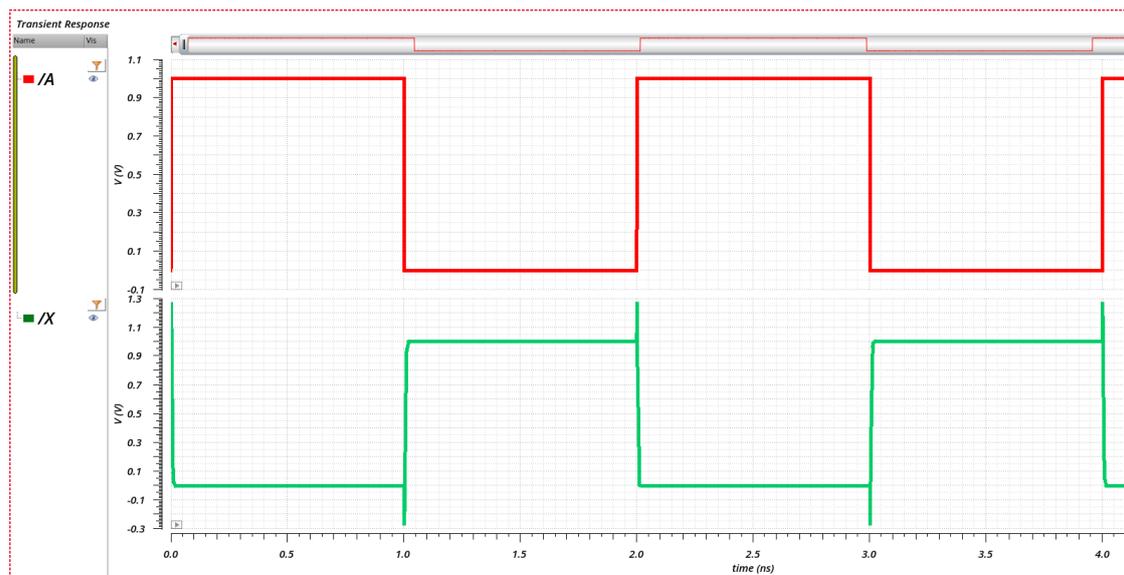


Figure 4.3: NOT Gate Waveform

Figure 4.1 shows the schematic of NOT Gate and Figure 4.2 shows its symbol. The symbol then goes through a testbench to determine its functionality. Figure 4.3 shows the NOT Gate Waveform output. This waveform shows that the NOT gate successfully inverted the input. However, there is a spike when inverting of the output occurred, possibly due to the parasitic capacitance.

4.1.1.2 NOR Gate

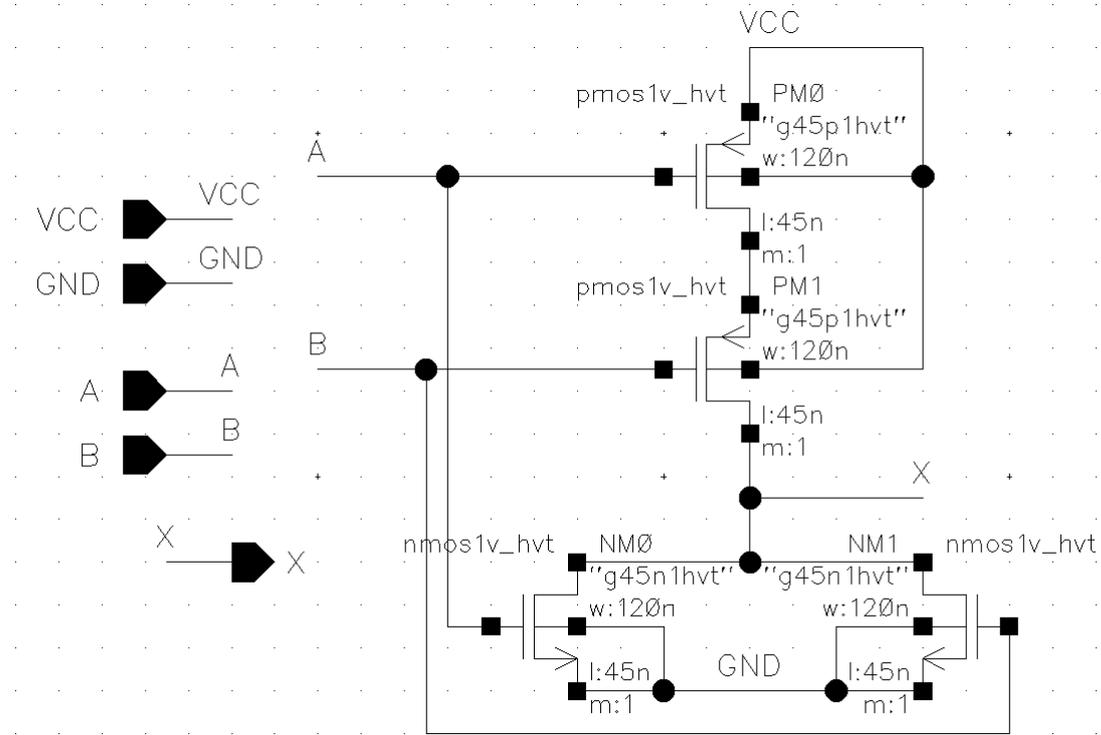


Figure 4.4: NOR Gate Schematic

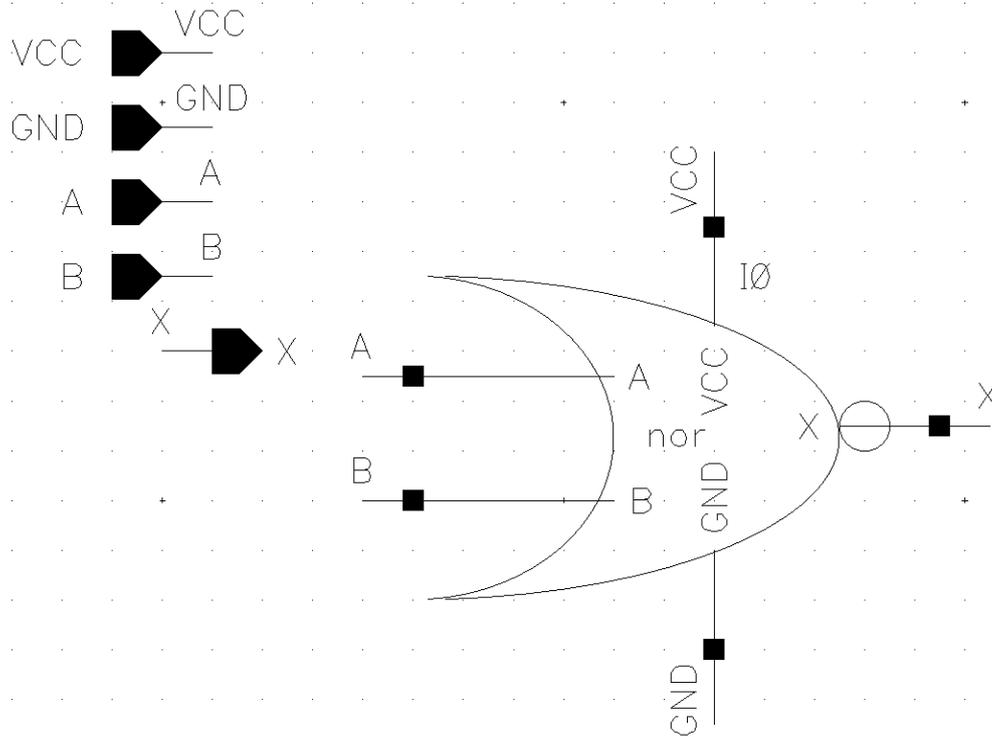


Figure 4.5: NOR Gate Symbol



Figure 4.6: NOR Gate Waveform

Figure 4.4 shows the schematic of NOR Gate and Figure 4.5 shows its symbol. The symbol then goes through a testbench to determine its functionality. Figure 4.6 shows the NOR Gate Waveform output. This waveform shows that the NOR gate successfully gives output 1 only when both of the 2 inputs are equals to 0 whereas the rest combinations gave output 0. However, there is a spike when the changes on output occurred, possibly due to the parasitic capacitance.

4.1.1.3 NAND Gate

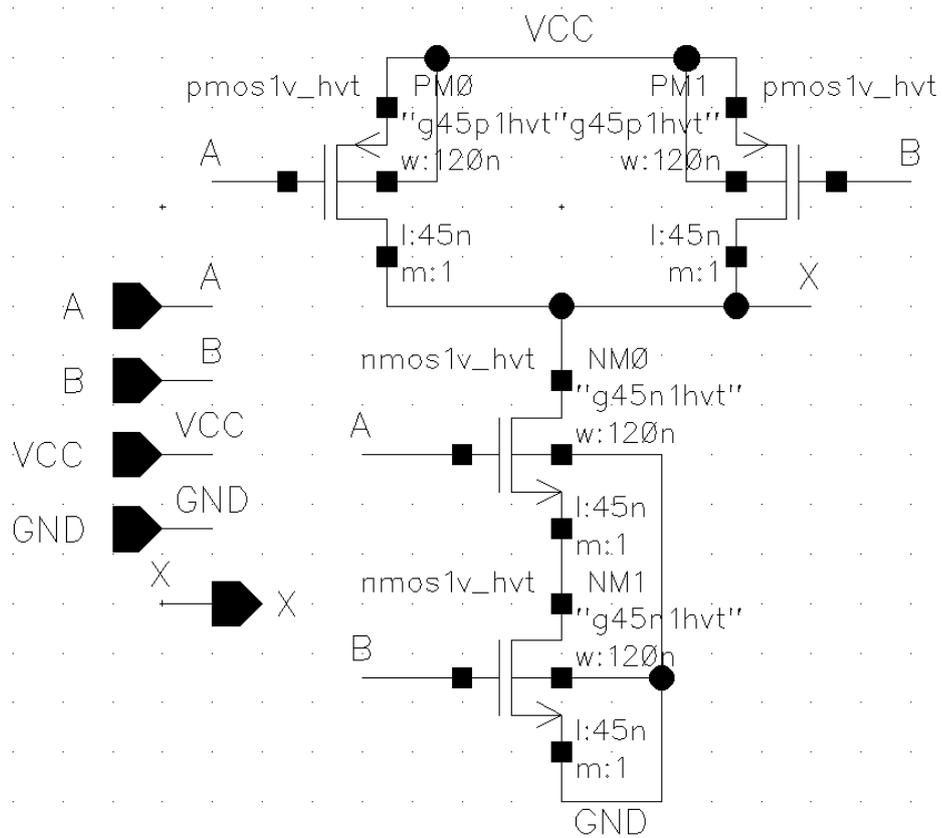


Figure 4.7: NAND Gate Schematic

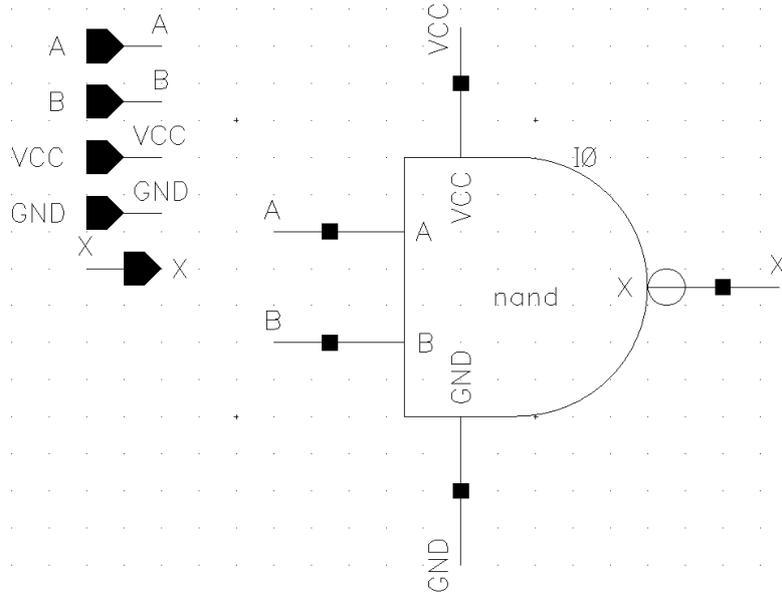


Figure 4.8: NAND Gate Symbol

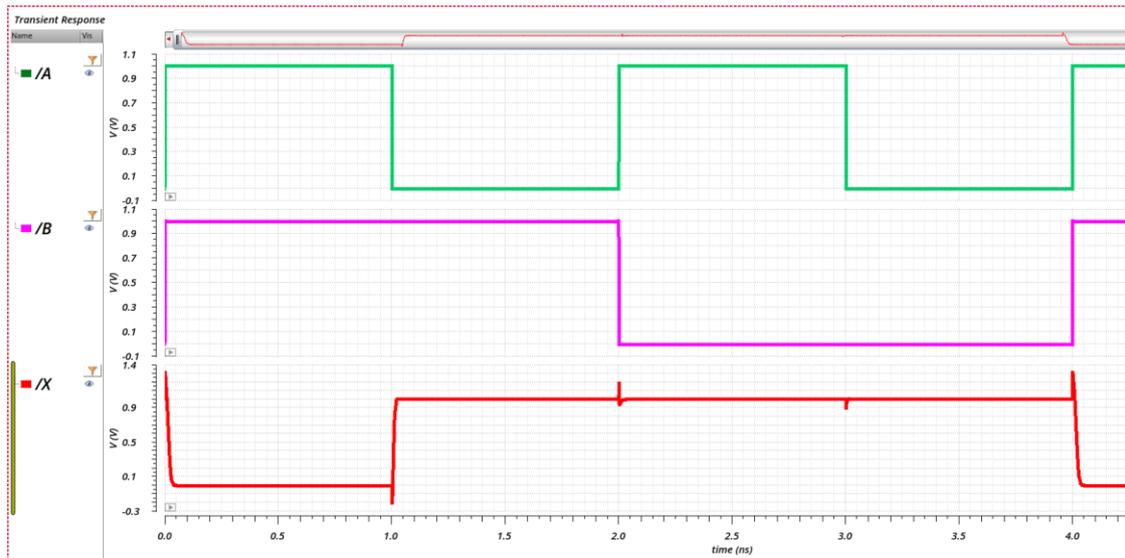


Figure 4.9: NAND Gate Waveform

Figure 4.7 shows the schematic of NAND Gate and Figure 4.8 shows its symbol. The symbol then goes through a testbench to determine its functionality. Figure 4.9 shows the NAND Gate Waveform output. This waveform shows that the NAND gate successfully gives output 0 only when both of the 2 inputs are equal to 1, whereas the rest combinations gave output 1. However, there is a spike when the changes in output occurred, possibly due to the parasitic capacitance.

4.1.1.4 OR Gate

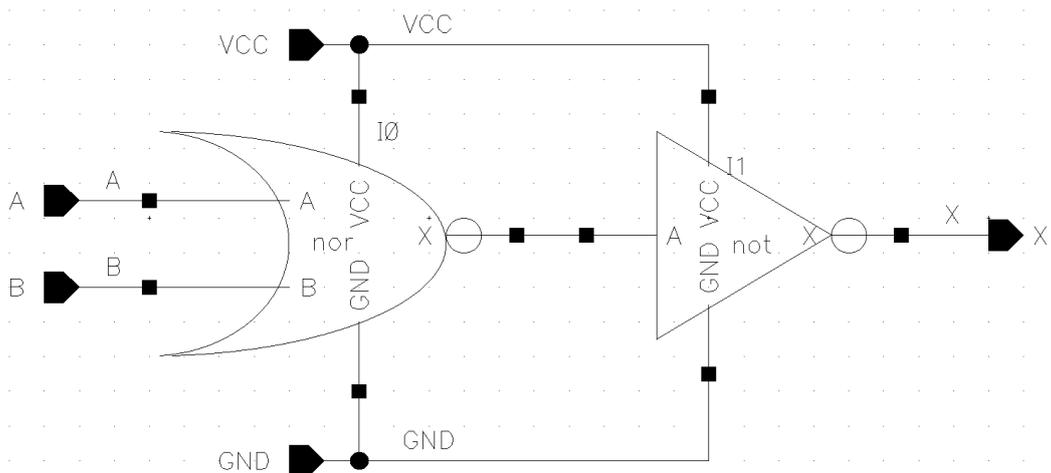


Figure 4.10: OR Gate Schematic

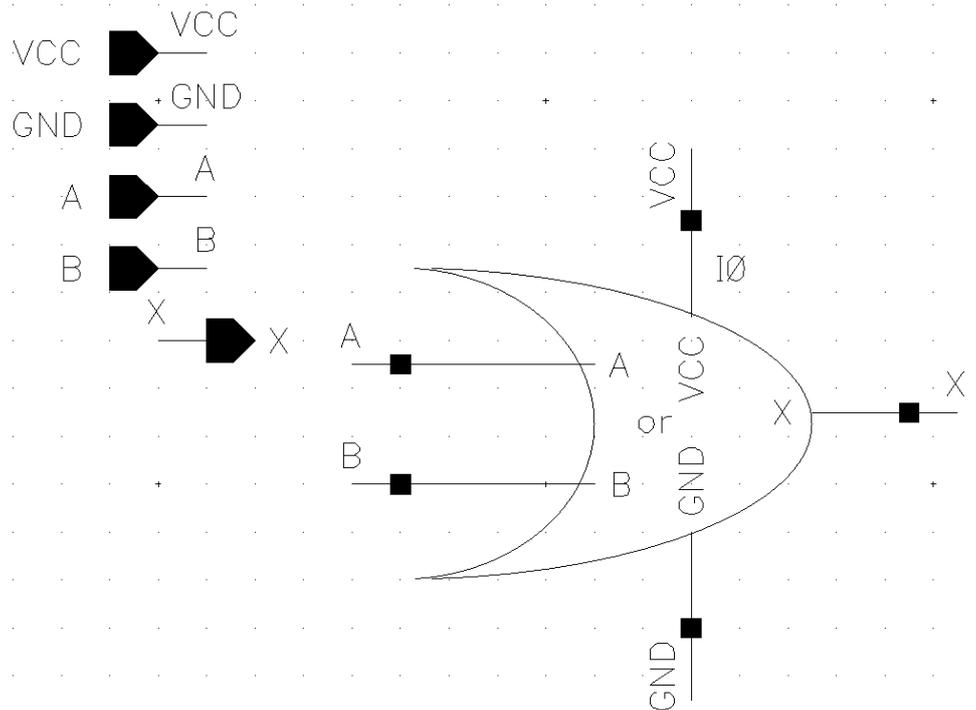


Figure 4.11: OR Gate Symbol



Figure 4.12: OR Gate Waveform

Figure 4.10 shows the schematic of OR Gate and Figure 4.11 shows its symbol. The symbol then goes through a testbench to determine its functionality. Figure 4.12 shows the NOR Gate Waveform output. This waveform shows that the OR gate successfully gives output 0 only when both of the 2 inputs are equal to 0 whereas the rest combinations gave output 1. The outputs of the OR gate are actually the inverted value of the NOR gate.

4.1.1.5 AND Gate

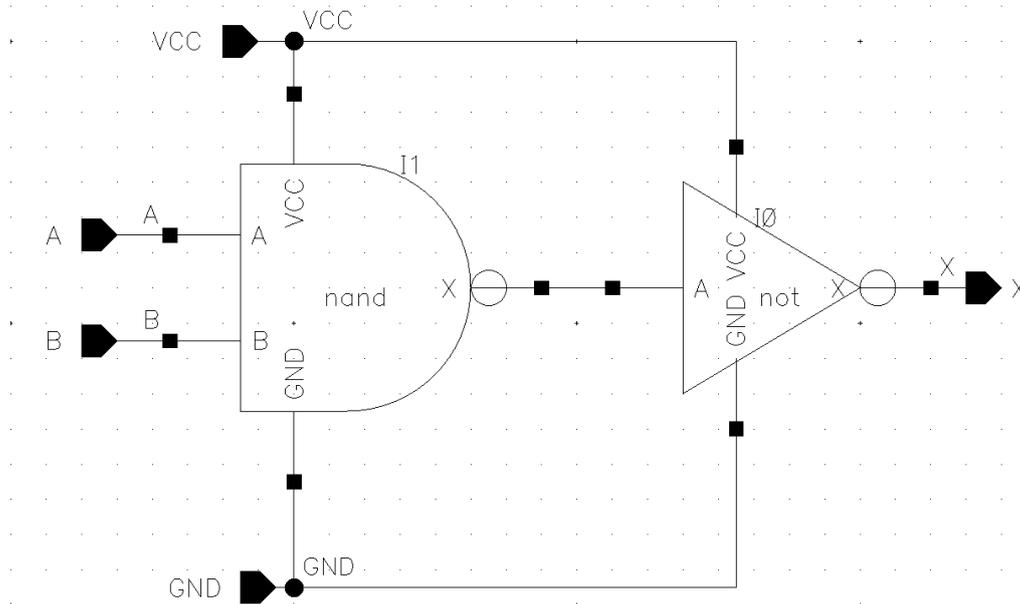


Figure 4.13: AND Gate Schematic

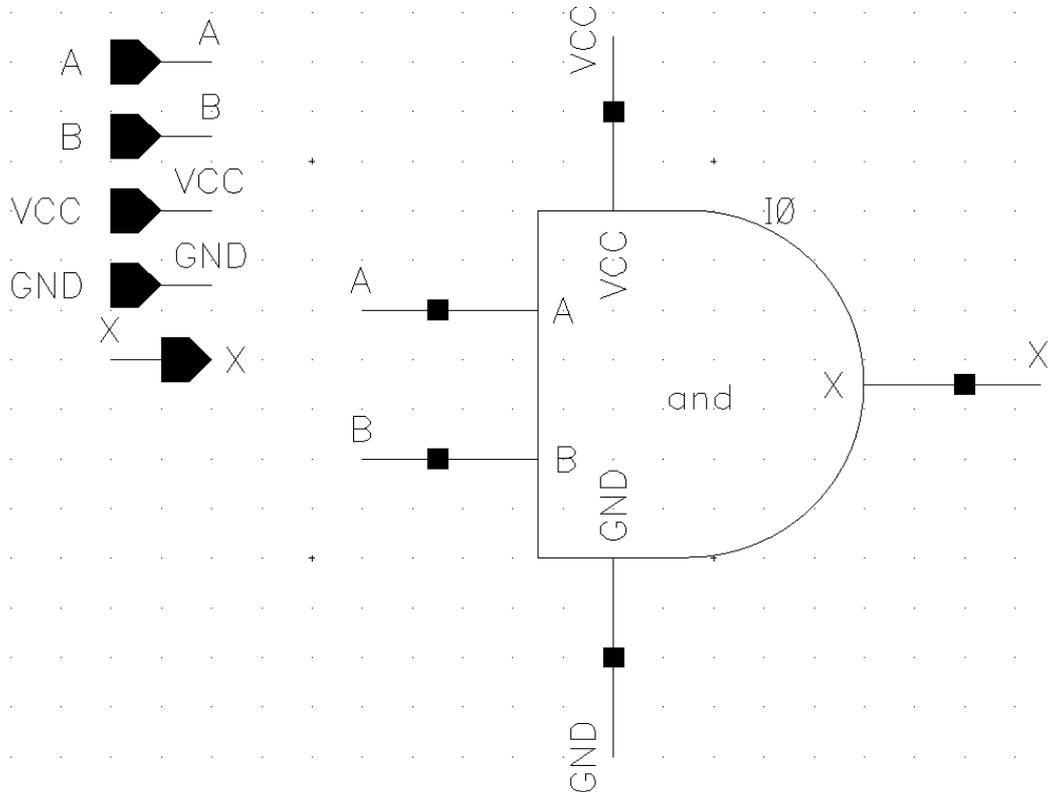


Figure 4.14: AND Gate Symbol



Figure 4.15: AND Gate Waveform

Figure 4.13 shows the schematic of AND Gate and Figure 4.14 shows its symbol. The symbol then goes through a testbench to determine its functionality. Figure 4.15 shows the AND Gate Waveform output. This waveform shows that the AND gate successfully gives output 1 only when both of the 2 inputs are equal to 1 whereas the rest combinations gave output 0. The output of the AND gate is actually the inverted value of the NAND gate.

4.1.1.6 XOR Gate

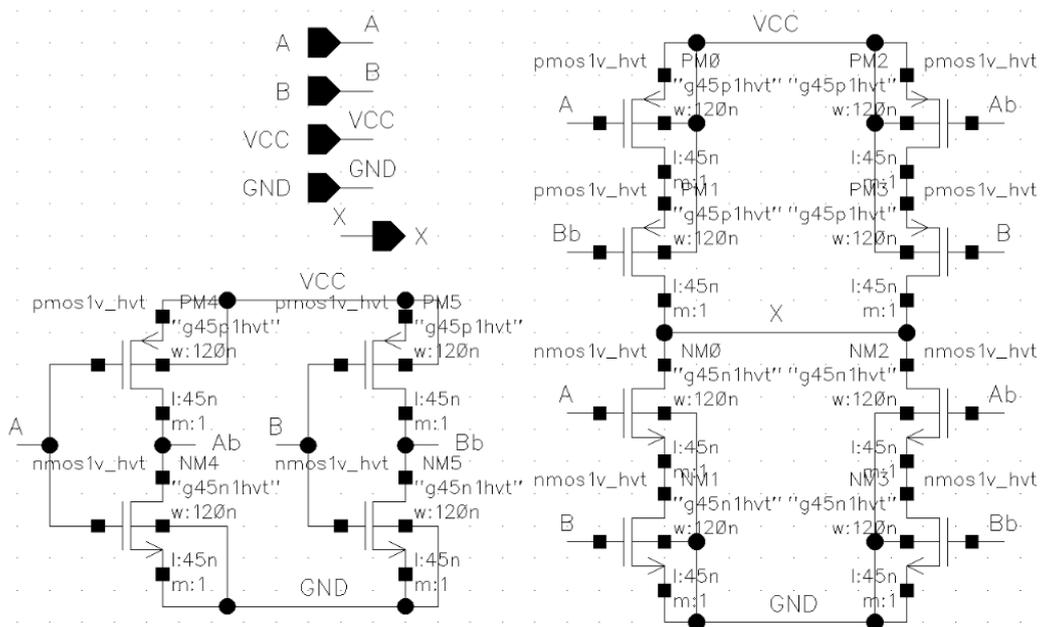


Figure 4.16: XOR Gate Schematic

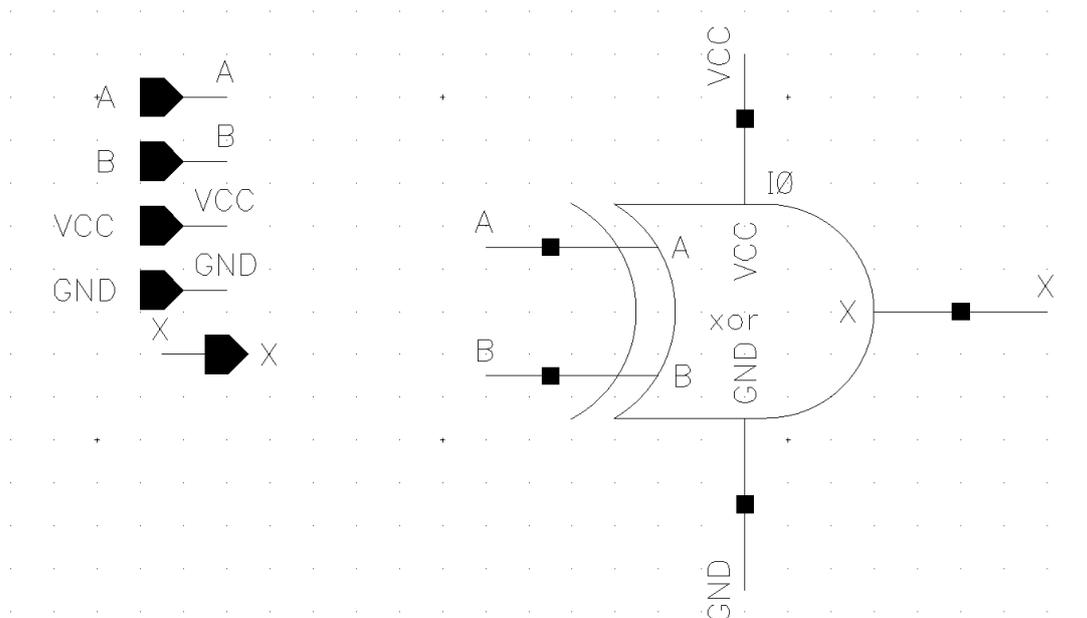


Figure 4.17: XOR Gate Symbol

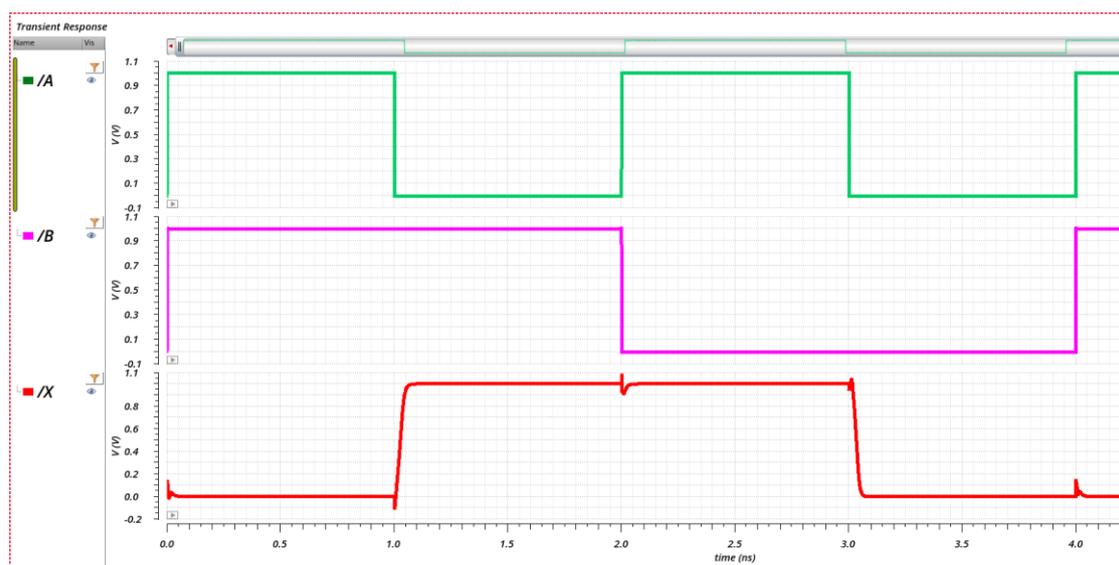


Figure 4.18: XOR Gate Waveform

Figure 4.16 shows the schematic of XOR Gate and Figure 4.17 shows its symbol. The symbol then goes through a testbench to determine its functionality. Figure 4.18 shows the XOR Gate Waveform output. This waveform shows that the XOR gate successfully gives output 1 only when both of the 2 inputs are different whereas the combinations of the same input value gave output 0.

4.1.1.7 XNOR Gate

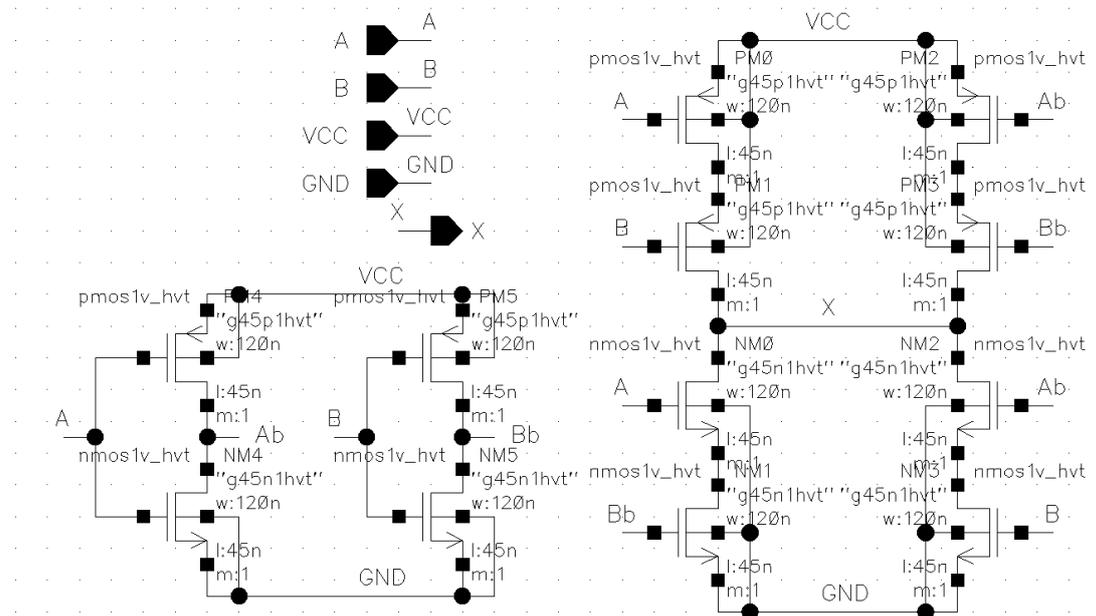


Figure 4.19: XNOR Gate Schematic

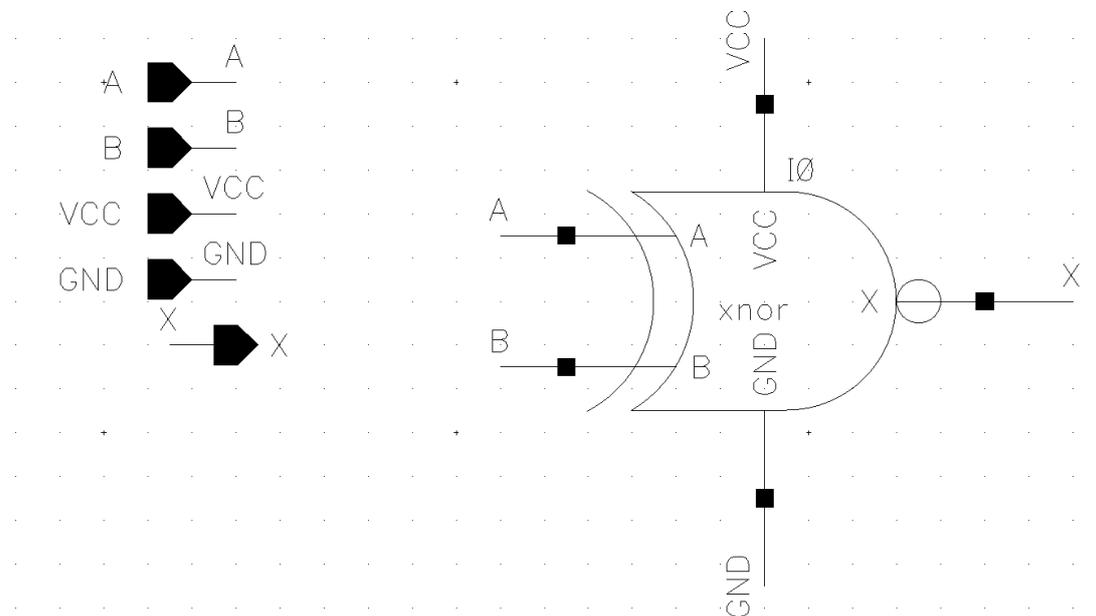


Figure 4.20: XNOR Gate Symbol

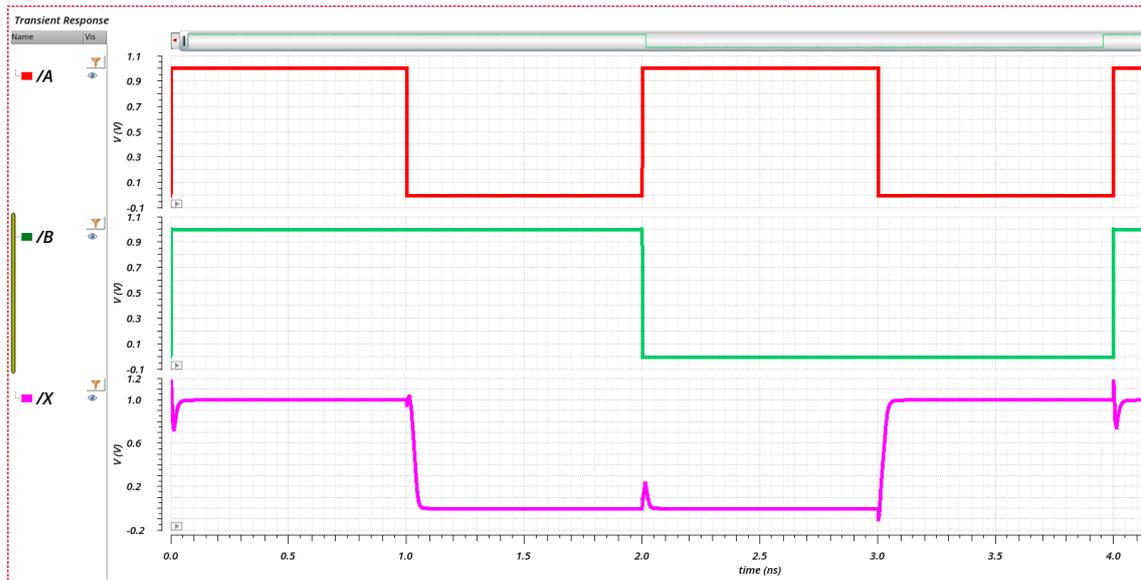
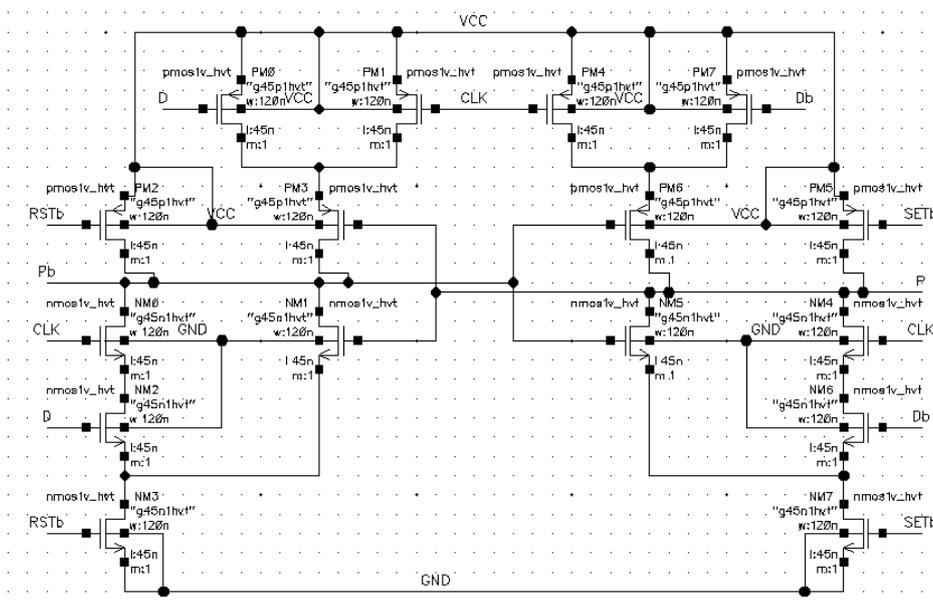


Figure 4.21: XNOR Gate Waveform

Figure 4.19 shows the schematic of XNOR Gate and Figure 4.20 shows its symbol. The symbol then goes through a testbench to determine its functionality. Figure 4.21 shows the XNOR Gate Waveform output. This waveform shows that the XNOR gate successfully gives output 0 only when both of the 2 inputs are different whereas the combinations of the same input value gave output 1. The output of the XNOR gate is actually the inverted value of the XOR gate.

4.1.1.8 CMOS DFF



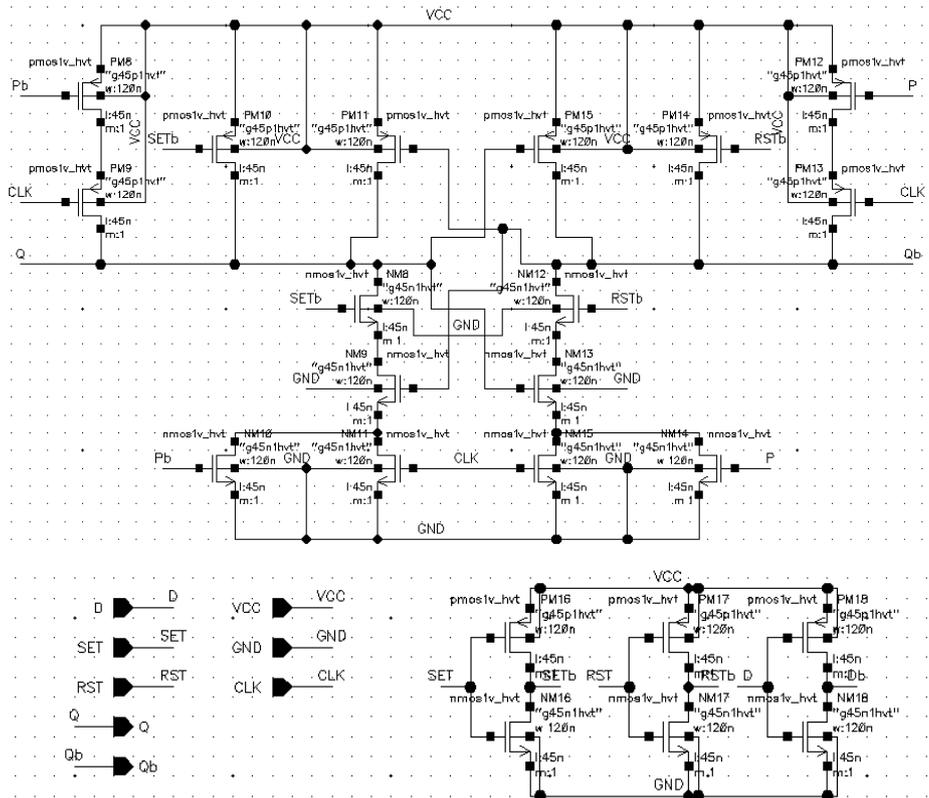


Figure 4.22: CMOS DFF Schematic

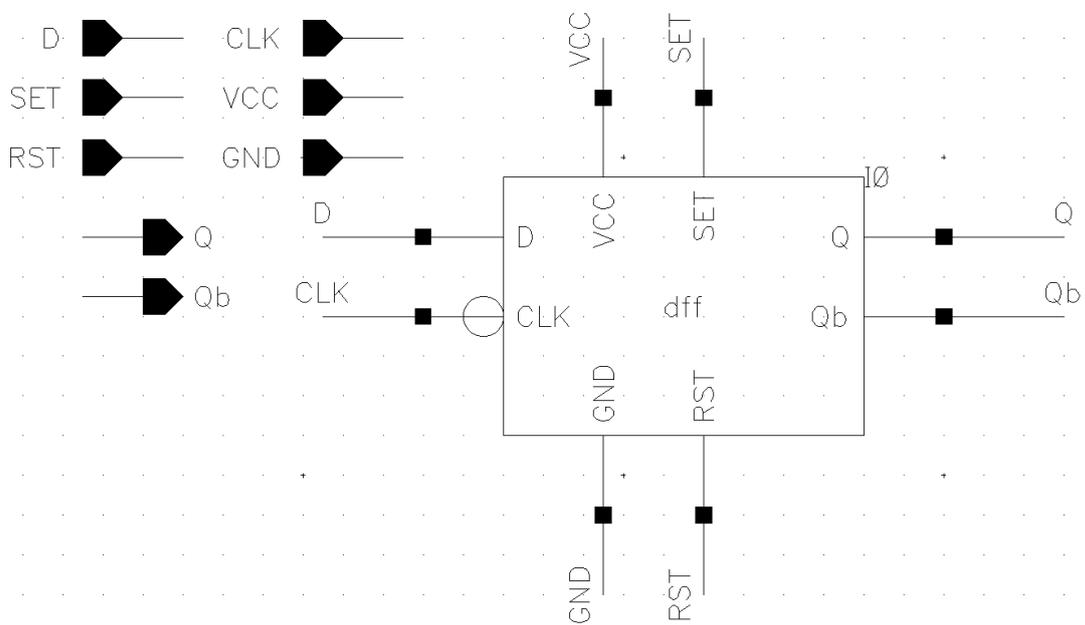


Figure 4.23: CMOS DFF Symbol

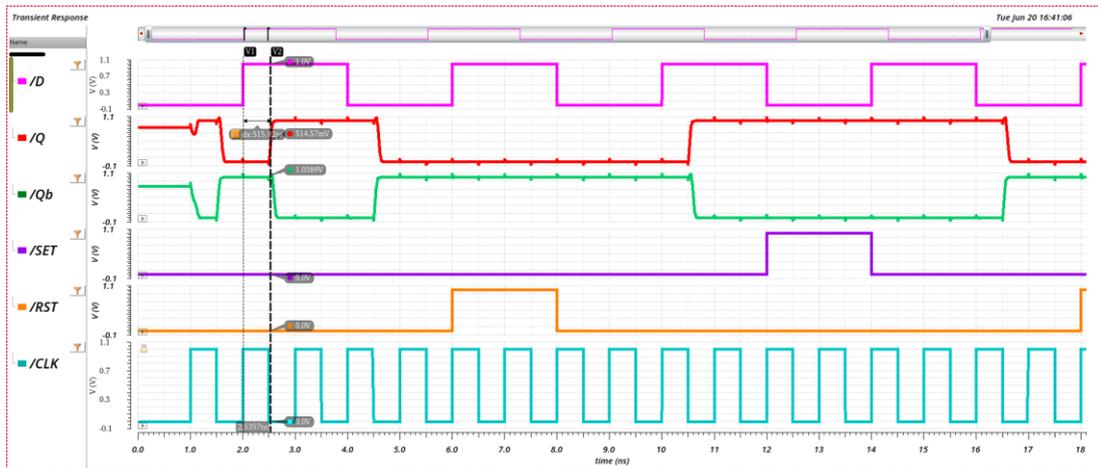


Figure 4.24: CMOS DFF Waveform

Figure 4.22 shows the schematic of CMOS DFF and Figure 4.23 shows its symbol. The symbol then goes through a testbench to determine its functionality. Figure 4.24 shows the CMOS DFF Waveform output. This waveform shows that the CMOS DFF successfully behaves accordingly with the truth table of Table 2.2. However, the output is delayed by approximately 515 ns due to the DFF is a negative edge clock device.

4.1.1.9 2:1 Multiplexer

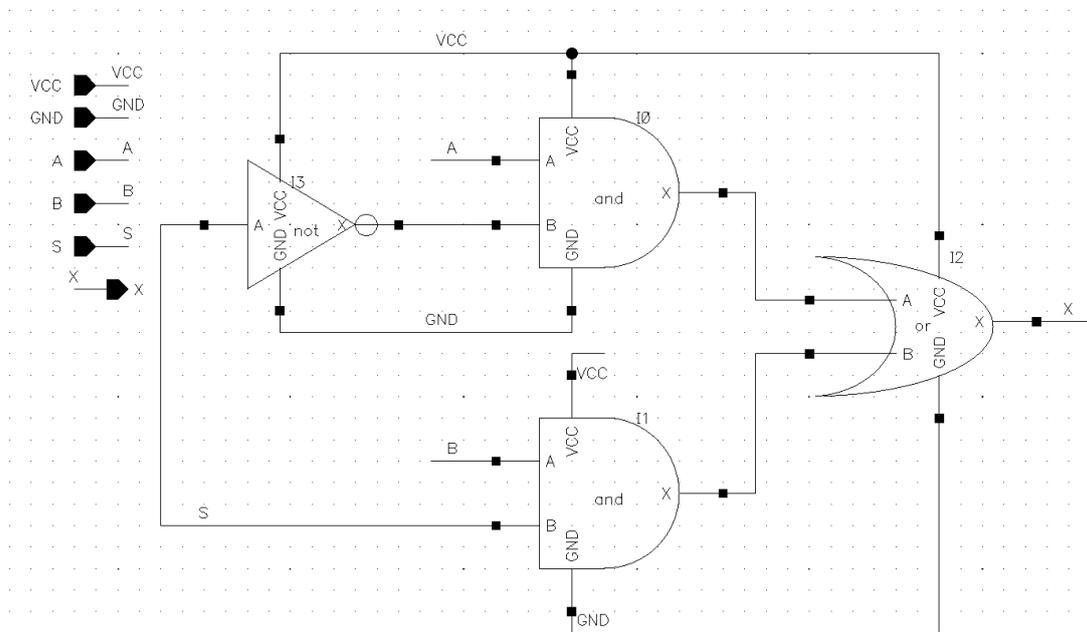


Figure 4.25: 2:1 Multiplexer Schematic

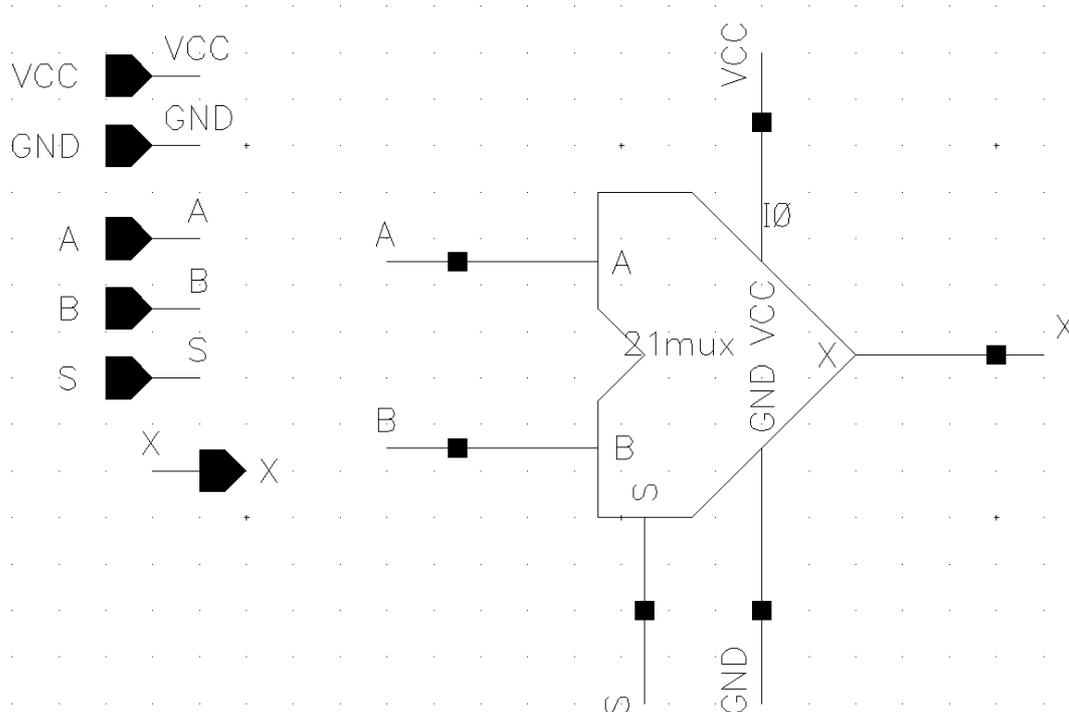


Figure 4.26: 2:1 Multiplexer Symbol

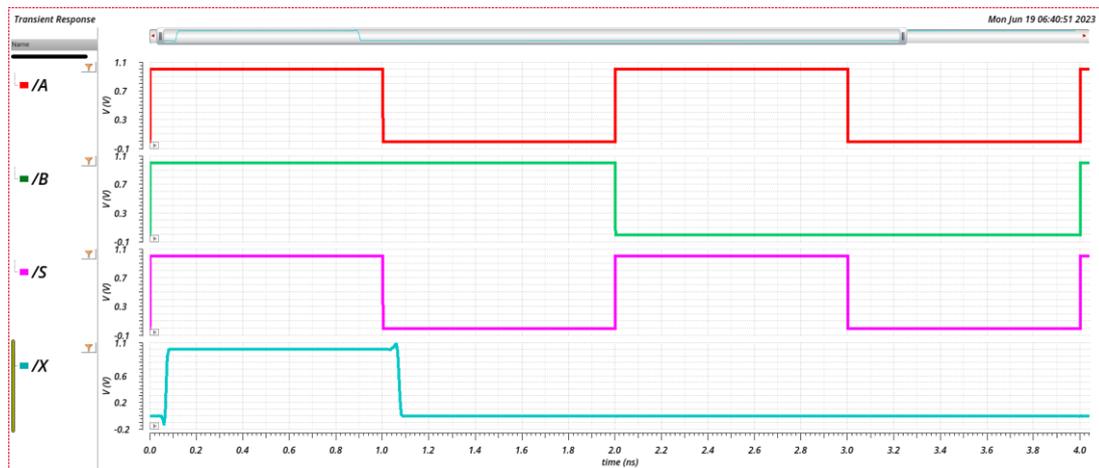


Figure 4.27: 2:1 Multiplexer Waveform

Figure 4.25 shows the schematic of 2:1 Multiplexer and Figure 4.26 shows its symbol. The symbol then goes through a testbench to determine its functionality. Figure 4.27 shows the 2:1 Multiplexer Waveform output. This waveform shows that the 2:1 Multiplexer successfully gives output based on the selector. When Selector = 0, the output would be A, and when Selector = 1, the output would be B. However, there is a slight time delay of 0.2 ns at the output possibly due to propagation delay.

4.1.1.10 Buffer Cell

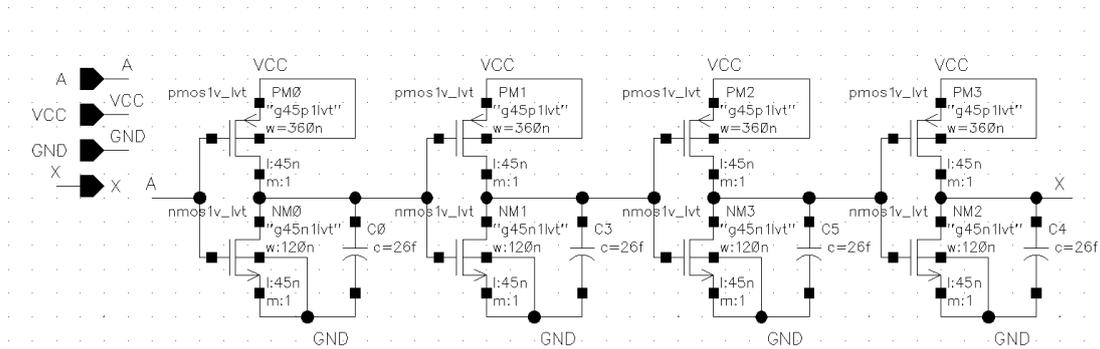


Figure 4.28: Buffer Cell Schematic

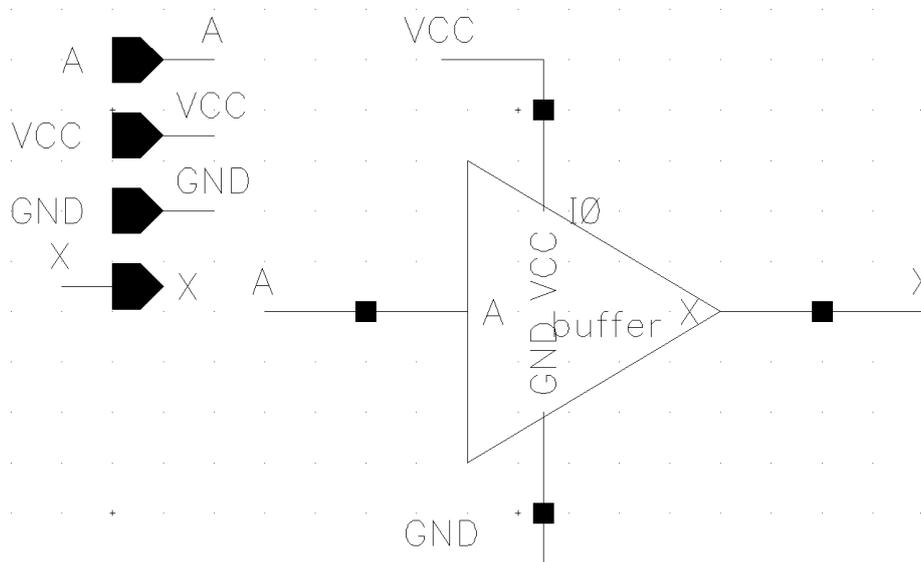


Figure 4.29: Buffer Cell Symbol

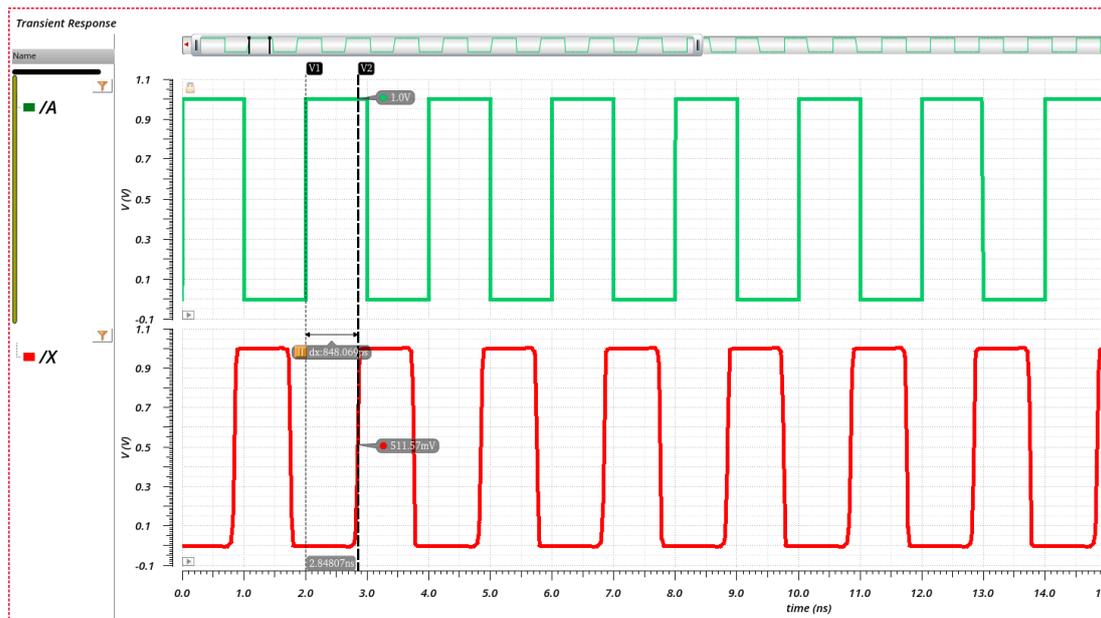


Figure 4.30: Buffer Cell Waveform

Figure 4.28 shows the schematic of Buffer Cell and Figure 4.29 shows its symbol. The symbol then goes through a testbench to determine its functionality. Figure 4.30 shows the Buffer Cell Waveform output. This waveform shows that the Buffer Cell successfully gives output that is delayed by half of the clock cycle, approximately 848 ns apart. This Buffer Cell is a series of chain inverters.

4.1.1.11 Analog Comparator

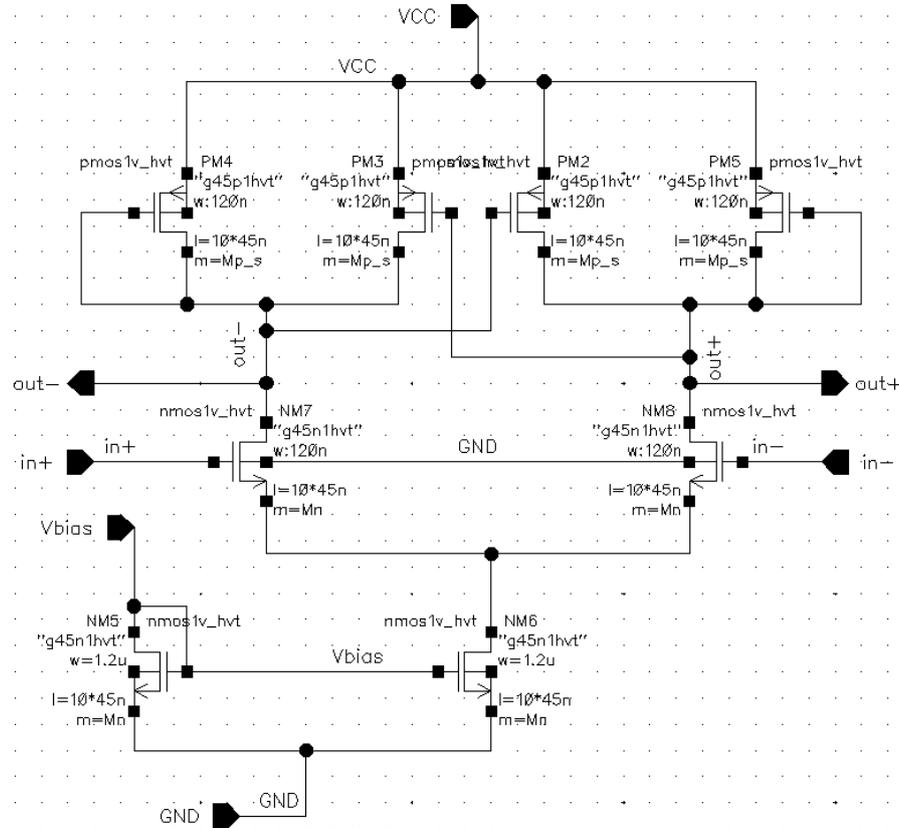


Figure 4.31: StrongArm Latch Schematic

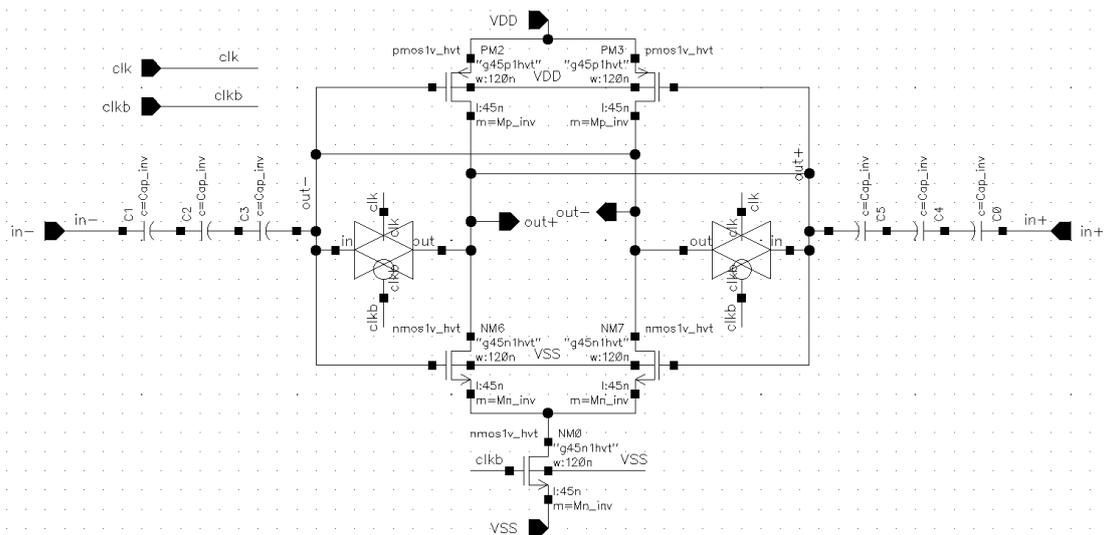


Figure 4.32: RS Latch Schematic

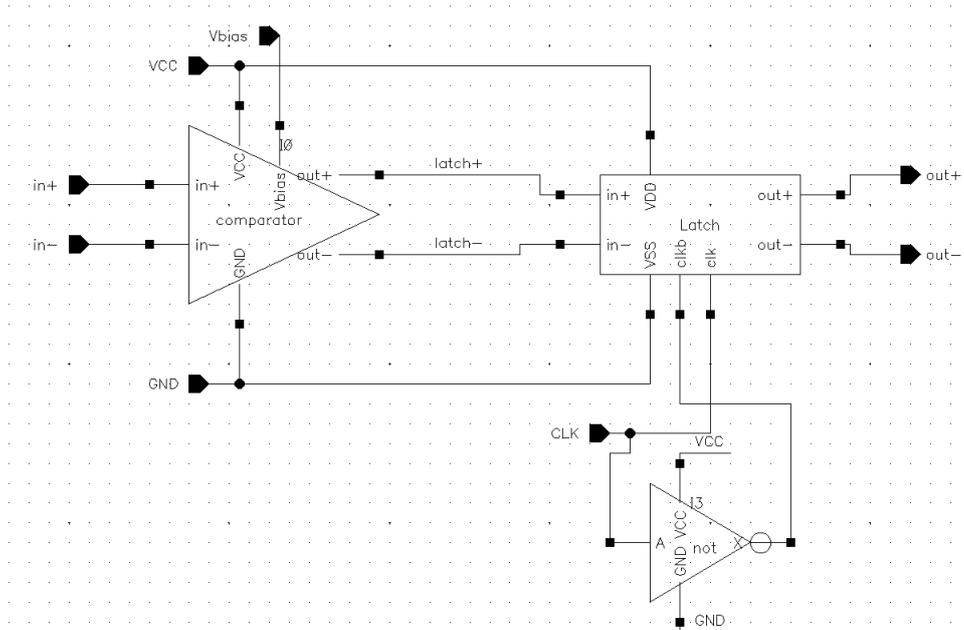


Figure 4.33: Analog Comparator Schematic

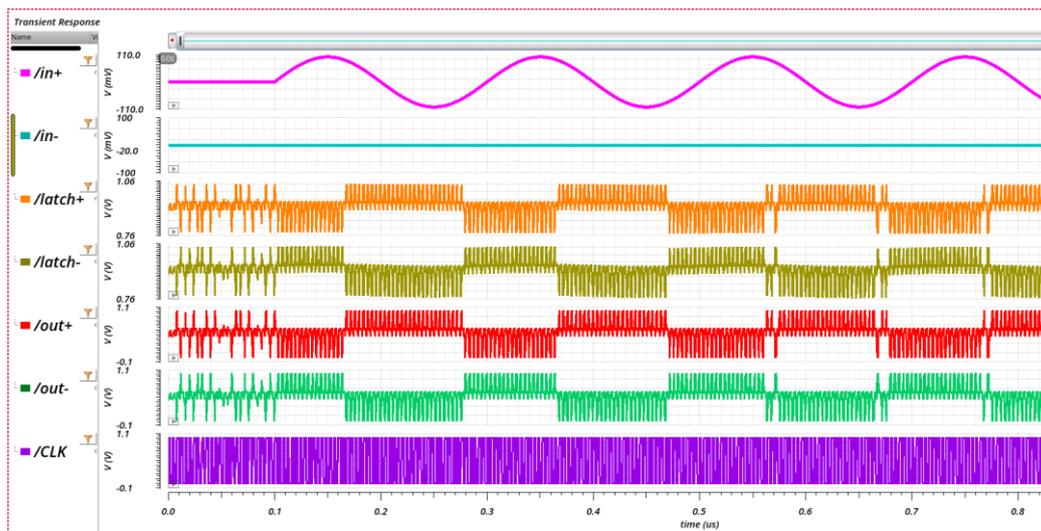


Figure 4.34: Analog Comparator Waveform

Figure 4.31 shows the schematic of StrongArm Latch and Figure 4.32 shows the schematic of RS Latch. The StrongArm Latch and the RS Latch will be combined to become a macro known as Analog Comparator as shown in Figure 4.33. The macro then goes through a testbench to determine its functionality. Figure 4.34 shows the Analog Comparator Waveform output. This waveform shows that the Analog Comparator successfully gave an output of strong '1' when analog input in+ is greater than analog input in- and gave an output of strong '0' when analog input in+ is lesser than analog input in-.