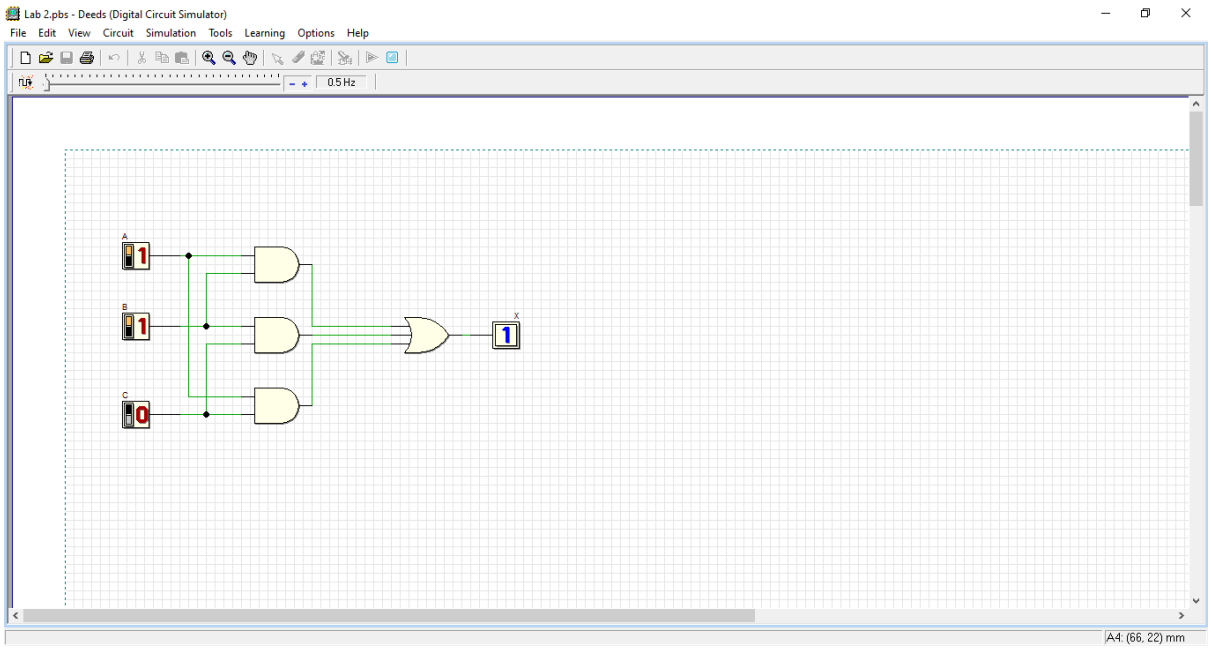
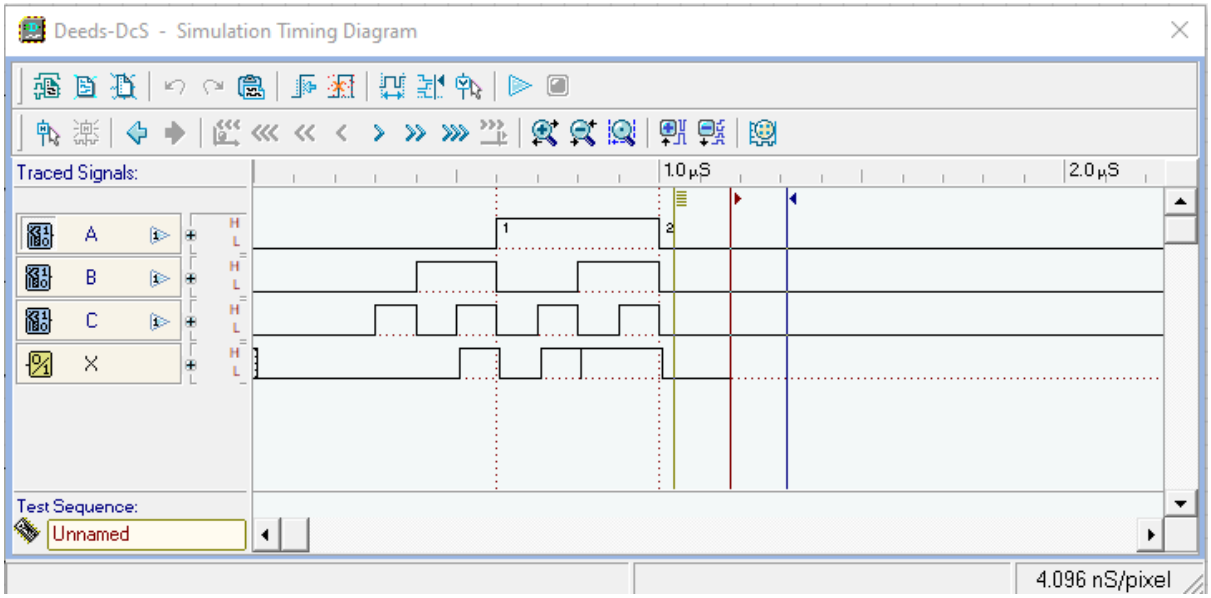
PART 1

Circuit (i)

Logic circuit

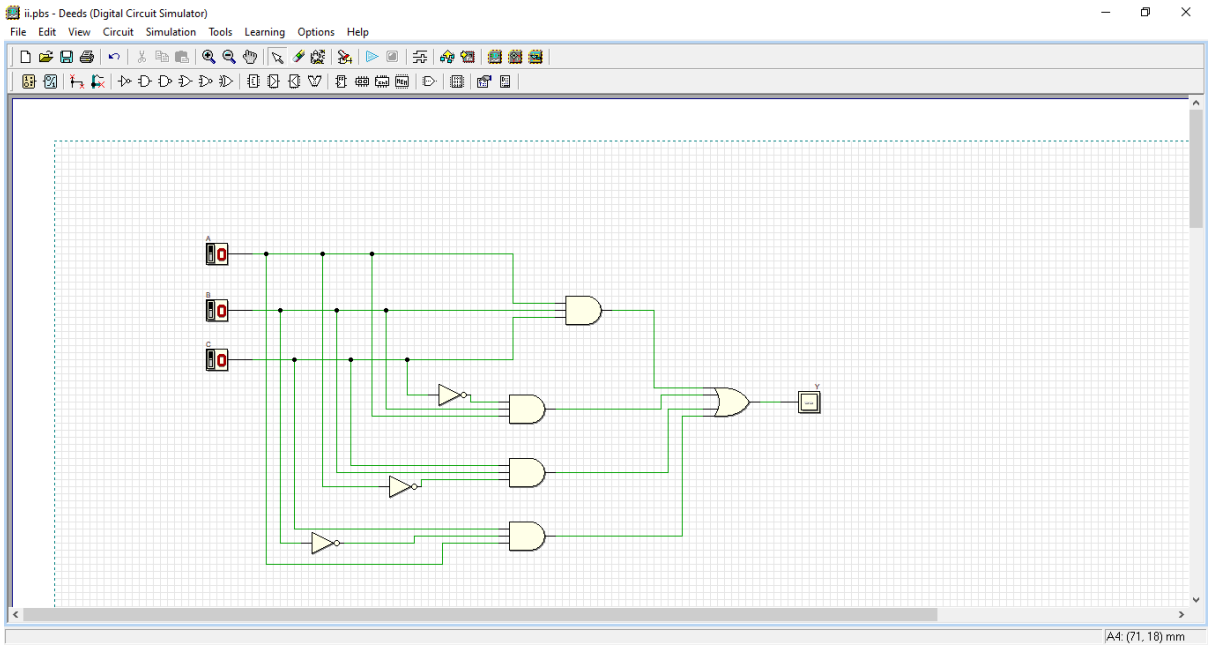


Timing diagram

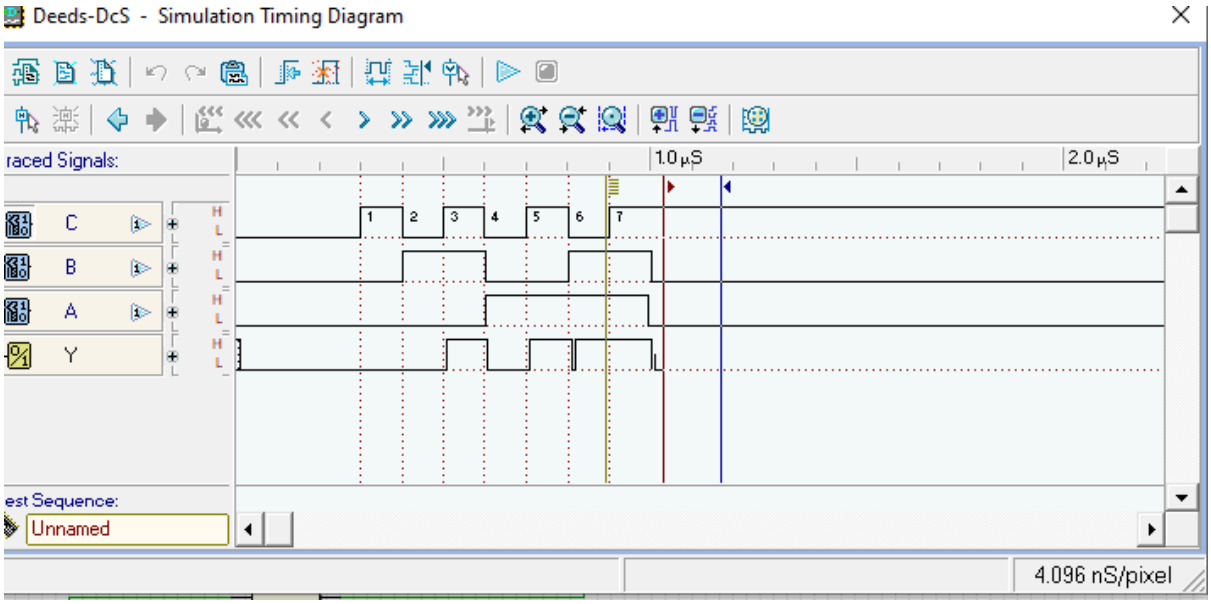


Circuit (ii)

Logic gate

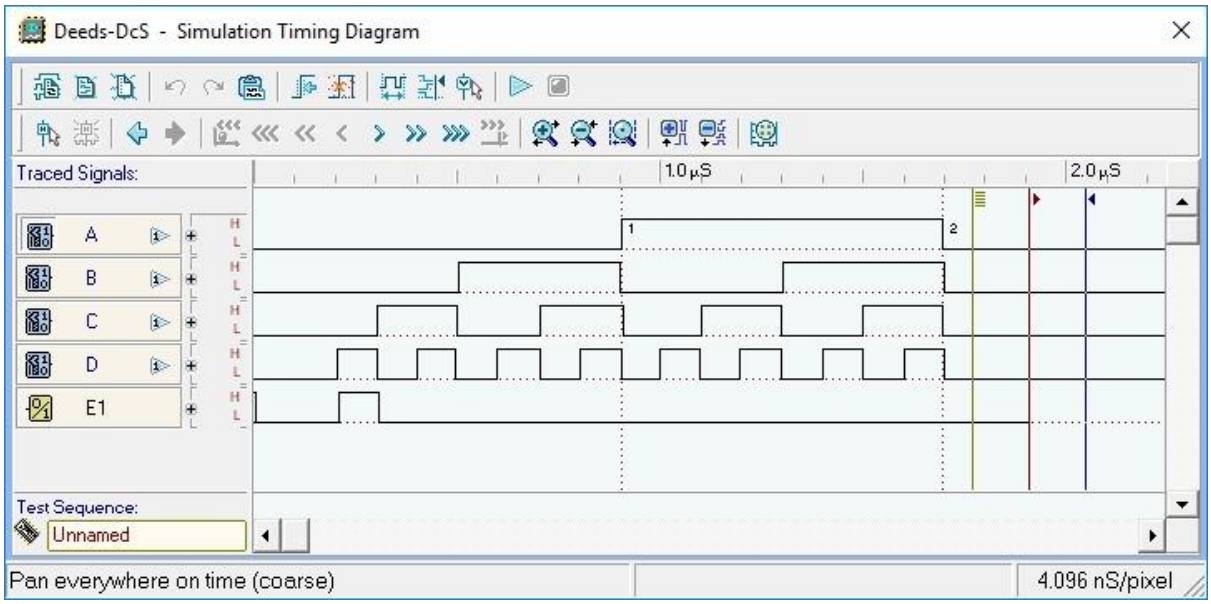


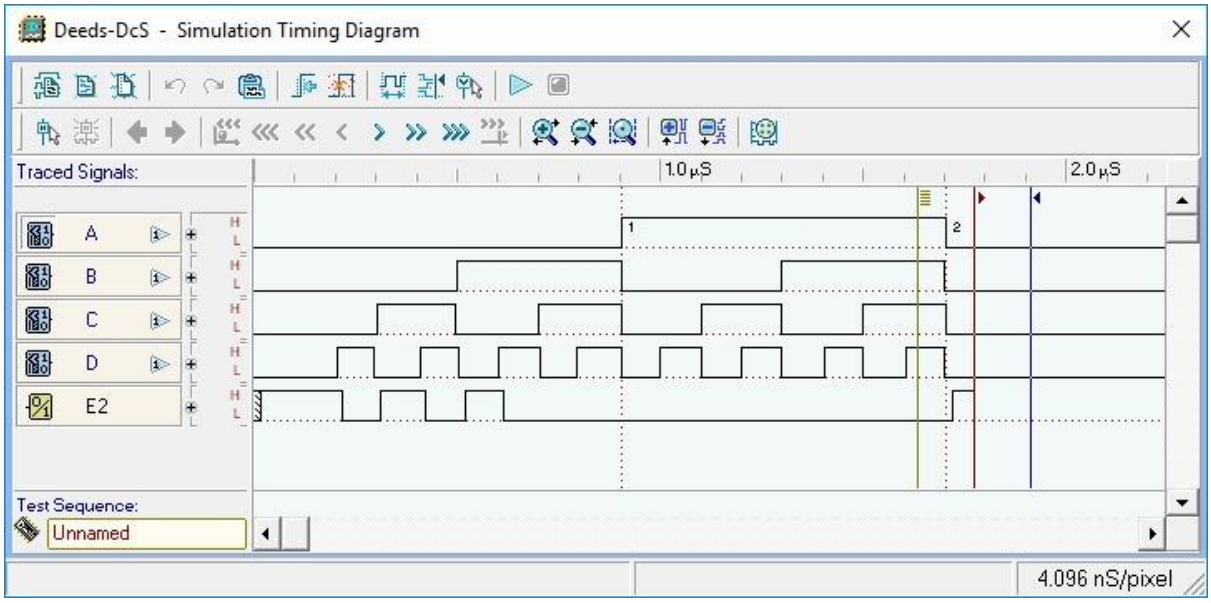
Timing diagram

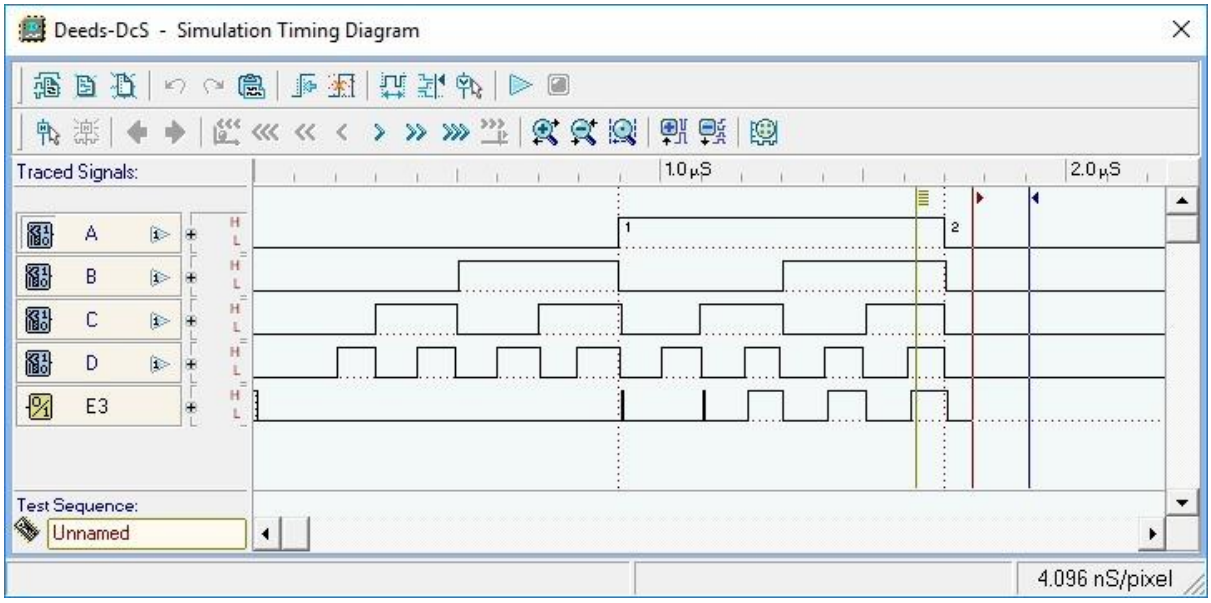


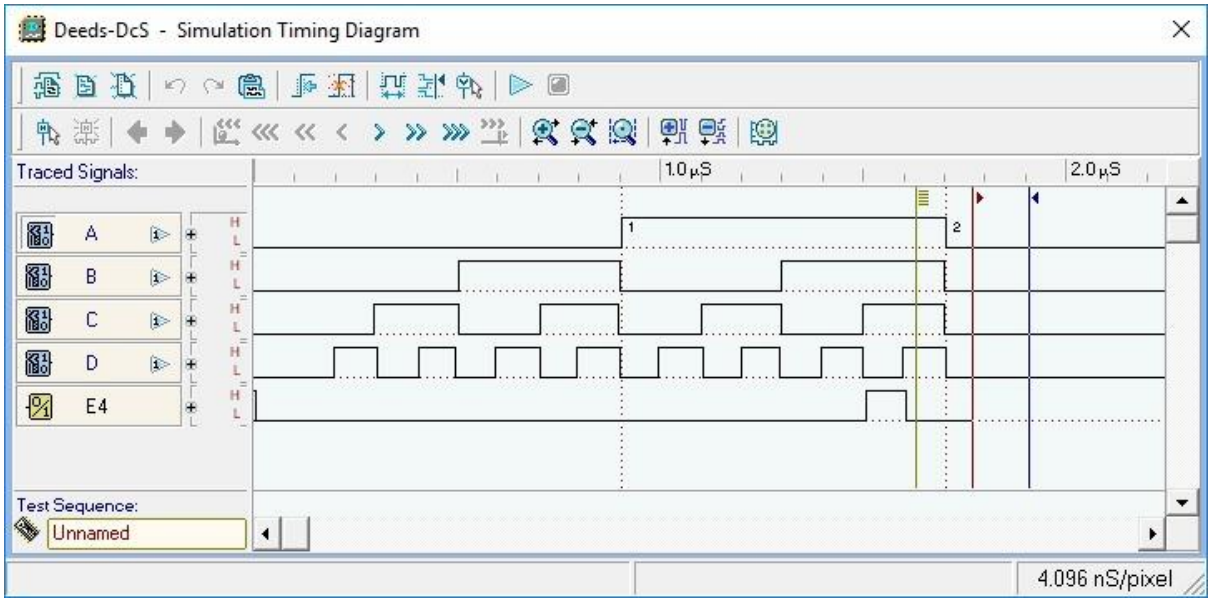
PART 2

Timing diagram using deeds circuit, E1, E2, E3, and E4.






Deeds-DcS - Simulation Timing Diagram
Traced Signals:
1.0 µS
2.0 µS
A
B
C
D
E3
Test Sequence:
Unnamed
4.096 nS/pixel


Deeds-DcS - Simulation Timing Diagram
Traced Signals:
1.0 µS
2.0 µS
A
B
C
D
E4
Test Sequence:
Unnamed
4.096 nS/pixel