Department of Computer Science
Faculty of Computing
UNIVERSITI TEKNOLOGI MALAYSIA

SUBJECT NAME: **DIGITAL LOGIC**

SUBJECT CODE: **SECR1013-01**

SEMESTER: **2021/2022**

LAB TITLE: **LAB 1: COMBINATIONAL LOGIC**

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SUBMITTED DATE: _____

COMMENTS:

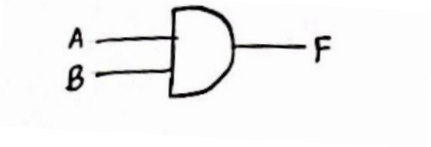
MARKS:

D. Preliminary Work

1. Draw a symbol, determine the IC number and produce a truth table for the following gate.

AND

Symbol:



IC Number: 7408

Truth Table 1

Input		Output
A	B	F
0	0	0
0	1	0
1	0	0
1	1	1

NAND

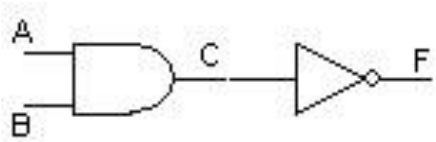
Symbol:

IC Number:7400

Truth Table 2

Input		Output
A	B	F
0	0	1
0	1	1
1	0	1
1	1	0

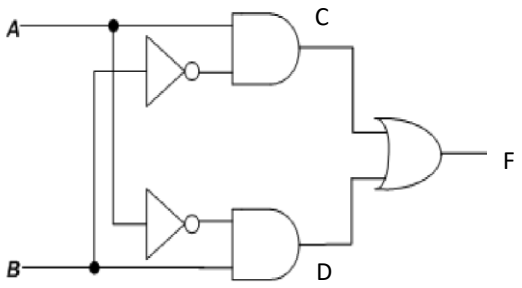
2. Complete the truth table for the following circuit.



Truth Table 3

A	B	C	D
0	0	0	1
0	1	0	1
1	0	0	1
1	1	1	0

3. Write the Boolean expression for output C, D and F in the following circuit.



C = $A\bar{B}$

D = $\bar{A}B$

F = $A\bar{B} + \bar{A}B$

4. Complete the truth table for the circuit in (3) based on the Boolean expression produced for C, D and F.

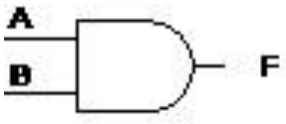
Truth Table 4

A	B	C	D	F
0	0	0	0	0
0	1	0	1	1
1	0	1	0	1
1	1	0	0	0

E. Laboratory Work

Part 1

1. Construct Circuit 1 on the breadboard. Connect all inputs (A, B) to a switch and output F to LEDs.



Truth Table 5

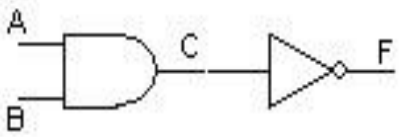
Input		Output
A	B	F
0	0	0
0	1	0
1	0	0
1	1	1

2. Test circuit 1 and fill in Truth Table 5 for the circuit response to all possible input combinations. The Truth Table 5 should match the Truth Table 1 prepared in the Preliminary Work.

Fully Completed ☐ *Partially Completed* ☐ *Checked by:* _____

Part 2

3. Construct Circuit 2 on the breadboard. Connect all inputs (A, B) to a switch and output F to LEDs.



Truth Table 6

A	B	C	F
0	0	0	1
0	1	0	1
1	0	0	1
1	1	1	0

4. Test Circuit 2, fill in Truth Table 6, for the circuit response to all possible input combinations.
5. Compare Truth Table 6 to Truth Table 2. What conclusion can you make?

Truth Table 6 matches Truth Table 2. Both logic circuits are equivalent.

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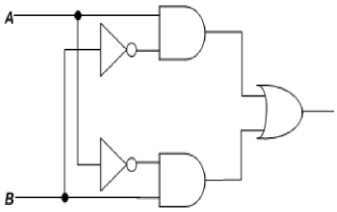
Part 3

6. Construct circuit 3 on the breadboard. Connect all inputs (A, B) to a switch and output C, D and F to LEDs.



Truth Table 7

A	B	C	D	F
0	0	0	0	0
0	1	0	1	1
1	0	1	0	1
1	1	0	0	0

7. Test Circuit 3, fill in Truth Table 7 for the circuit outputs (C, D and F) for all possible input combinations.

8. What single gate does Circuit 3 represent?

XOR Gate

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