School/Faculty	Computing/Engineering	Page:	1 of 5
Programme Name	Bachelor of Computer Science (Computer Networks & Security)		
Course code:	SECR1013	Academic Session/Semester:	2021/2022-1
Course name:	DIGITAL LOGIC	Pre/co requisite:	NIL
Credit hours:	3		

COURSE OUTLINE

Course synopsis	Digital electronics is the foundation of all microprocessor-based systems found in computers, robots, automobiles, and industrial control systems. This course introduces the students to digital electronics and provides a broad overview of many important concepts, components, and tools. Students will get up-to-date coverage of digital fundamentals-from basic concepts to programmable logic devices. Laboratory experiments provide hands-on experience with the simulator software, actual devices and circuits studied in the classroom
Course coordinator	Nur Haliza Binti Abdul Wahab

Course lecturer(s)	Name	Section	Office	E-mail @utm.my
	Dr. Mohd Fo'ad bin Rohani	01	N28-347-02	foad
	Dr. Haswadi Bin Hasan	02 & 07	N28-347-06	haswadi
	Dr. Nur Haliza binti Abd Wahab	03, 06, & 09	N28A-02-11	nur.haliza
	Ms Marina binti Md Arshad	04 & 05	N28-347-08	marinama
	Dr. Ismail Fauzi Bin Isnin	08	N28A-	ismailfauzi
	Dr. Nor Shahida Binti Hassan	15	Level 3, MJIIT KL	norshahida.kl

Mapping of the Course Learning Outcomes (CLO) to the Programme Learning Outcomes (PLO), Teaching & Learning (T&L) methods and Assessment methods:

No.	CLO	PLO (Code)	Weight (%)	Taxonomies and generic skills	T&L methods	*Assessment methods
CLO1	Apply the fundamentals of digital knowledge concept and numbering systems to digital logic circuits.	PLO1(KW)	15	C3	Lecture Tutorial	T1
CLO2	Design combinational logic circuits using logic gates and Boolean algebra.	PLO1(KW)	30	C4	Lecture Tutorial	T2
CLO3	Design sequential asynchronous and synchronous circuits using fundamentals of latches and flip-flops.	PLO1(KW)	30	C4	Lecture Tutorial	F
CLO4	Use the techniques, skills and digital logic tools in a successful lab exercise.	PLO2 (AP)	10.5	P3	Lab	L1, L2, L3,
CLO5	Design, implement and report on a digital logic circuit based on practical problems.	PLO3 (AP) PLO4(CS)	14.5	P5 CS1	Problem-based learning	L4, PR, GR D
*T – Test; Q – Quiz; HW – Homework; L – Lab, GR – Group Report; PR – Project; D - Demo, F – Final Exam etc.						

Prepared by:		Certified by:	
Name:	Dr. Mohd Fo'ad bin Rohani (Course Owner)	Name:	Professor Dr Md Asri bin Ngadi (Director of Computer Science)
Signature:		Signature:	
Date:	18 September 2021	Date:	

COURSE OUTLINE

Details on Innovative T&L practices:

No.	Type	Implementation
1.	Active learning	Conducted through in-class activities
2.	Project-based learning	Conducted through design project. Students in a group of 2 design projects that require digital logic solutions involving the design and verification using real devices. Compliance to the design specifications need to be given in the form of written reports and demo.

Weekly Schedule:

WEEK 1	**Class briefing** **Module 1: Digital Logic Overview** Digital and Analogue Quantities, Binary Digits, Logic Levels and Digital Waveforms, Introduction to Logic Operations, Overview of Logic Functions, Fixed-Function IC, Programmable Logic Device (PLD)
WEEK 2	**Module 2: Number Systems and Codes** Numbering System (Decimal, Binary, Octal and Hexadecimal), Number Conversion between Bases, Binary to Octal and Hexadecimal Conversion, Codes: BCD, GRAY, Parity, ASCII Arithmetic Operations: Integer (Unsigned, Signed Number) Operations: Addition and Subtraction
WEEK 3	**Module 3: Logic Gates** Inverter (NOT), AND, OR, NAND, NOR, XOR and XNOR Gates **(Lab 1)** Introduction to DEEDS
WEEK 4	**Module 4: Boolean Algebra and Logic Simplification** Laws and Rules of Boolean Algebra, DeMorgan's Theorem **(Test 1)**
WEEK 5 **WEEK 6**	Combinational Logic Representation (Boolean to Logic Circuit, Logic Circuit to Boolean, Boolean to Truth Table, Logic Circuit to Truth Table), Simplification Using Boolean Algebra, Standard Forms of Boolean Expressions (SOP and POS Form), Karnaugh Map (K-Map), K-Map Minimisation (SOP and POS), Don't Care Conditions
WEEK 7	**Module 5: Combinational Logic Circuit** Basic Combinational Logic Circuits (AND-OR, AND-OR-INVERT, XOR, XNOR), Universal Property of NAND and NOR, Dual Symbol, Design a Combinational Circuit **(Lab 2)**
WEEK 8	**MID SEMESTER BREAK**
WEEK 9	**Module 6: Functions of Combinational Logic** Basic and Parallel Binary Adders, Comparators, Decoders, Encoders, Multiplexer (Data Selector), Demultiplexer, Code Converter, Parity Generator/ Checker **(Test 2) Project (Part 1**
WEEK 10 **WEEK 11**	**Module 7: Latches, Flip-Flops and Timers** Latch (SR, Gated SR and Gated D), Flip-flop (SR, JK, D, T)
WEEK 12	**Module 8: Counters**

COURSE OUTLINE

WEEK 13	Types of Sequential Circuits, Counters, Design and Analysis of Asynchronous Counter, Operation (Up/Down, Truncated), Asynchronous Counter Decoder, Flip-flop Excitation Table, Design and Analysis of Synchronous Counter (Up/Down, Truncated), Counter for Arbitrary Sequences, Cascaded Counter, Analysis of Sequential Circuits (SR, JK, D, T)
WEEK 14	**Lab 3, Project (Part 2) – Group Report & Demo**
WEEK 15	**Module 9: Shift Register** Basic Shift Register Functions, SISO, SIPO, PISO, PIPO, Bidirectional Shift Register, Shift Register Counter (Ring and Johnson Counter)

Transferable skills (generic skills learned in course of study which can be useful and utilised in other settings):

Communication skills

Student learning time (SLT) details:

Distribution of course content	Teaching and Learning Activities						
	Guided Learning (Face to Face)				Guided Learning NF2F	Independent Learning NF2F	TOTAL SLT
CLO	**Lecture**	**Tutorial**	**Practical**	**Others**			
CLO 1	5	1			2	4	**12h**
CLO 2	13	2			4	16	**35h**
CLO 3	18	3			4	23	**48h**
CLO 4			8			1.5h	**9h 30m**
CLO 5			1.5	0.5		7	**8h**
Total SLT	**36**	**6**	**9.5**	**0.5**	**10**	**51.5**	**113h 30m**

Formative Assessment		PLO	Percentage	Total SLT
1	Lab 1 – 3 (CLO4)	PLO2 (AP)	3.5 x 3	As in CLO4 (6h)
2	Project Part 1 (CLO5)	PLO2 (AP)	3.5	As in CLO5 (2h)
3	Project Part 2 (CLO5)	PLO2 (AP) PLO4 (CS)	6 5	As in CLO5 (6h)
4	Test 1 (CLO1)	PLO1 (KW)	15	**1h 30m**
Summative Assessment			Percentage	Total SLT
1	Test 2 (CLO2)	PLO1 (KW)	25	**2h**
2	Final Exam (CLO2)	PLO1 (KW)	5	**30m**
3	Final Exam (CLO3)	PLO1 (KW)	30	**2h 30m**
Grand Total SLT				**120h**

COURSE OUTLINE

Special requirement to deliver the course (e.g: software, nursery, computer lab, simulation room):

Digital Logic Lab and Lab Assistant (TA)
Software: Deeds Software, WinCUPL software, Wellon software, Universal Programmer Hardware: Burner device, ETS5000, Integrated Circuits (IC), IC Tester, Coloured wire.

Learning resources:

Text book (if applicable)
Digital Logic (2018), School of Computing, Faculty of Engineering, UTMJB
Digital Logic Lab Manual (2021), School of Computing, Faculty of Engineering, UTMJB

Main references
Floyd, T.L., (2014), "Digital Fundamentals", 10th Edition, Prentice Hall, USA.

Additional references
Tocci, R.J., Widmer, N.S. and Moss, G.L, (2014), "Digital Systems", 11th Edition, Prentice Hall, USA.
Roth, C., (2014), "Fundamental of Logic Design", 7th Edition, Thomson Brooks, USA.

Online
http://elearning.utm.my

Academic honesty and plagiarism:

Assignments are individual tasks and NOT group activities (UNLESS EXPLICITLY INDICATED AS GROUP ACTIVITIES). Copying of work (texts, lab results etc.) from other students/groups or from other sources is not allowed. Brief quotations are allowed and then only if indicated as such. Existing texts should be reformulated with your own words used to explain what you have read. It is not acceptable to retype existing texts and just acknowledge the source as a reference. Be warned: students who submit copied work will obtain a mark of **zero** for the assignment and exams and disciplinary steps may be taken by the Faculty. It is also unacceptable to do somebody else's work, to lend your work to them or to make your work available to them to copy.

Other additional information (Course policy, any specific instruction etc.):

1. Attendance is compulsory and will be taken in every lecture session. Student with less than 80% of total attendance is not allowed to sit for final exam.
2. Students are required to behave and follow the University's dressing regulation and etiquette all the time.
3. Exercises and tutorial will be given in class and some may be taken for assessment. Students who do not do the exercise will lose the coursework marks for the exercise.
4. Assignments must be submitted on the due dates. Some points will be deducted for late submissions. Assignments submitted three days after the due date will not be accepted.
5. Make up exam will not be given, except to students who are sick and submit medical certificate confirmed by UTM panel doctors. Make up exam can only be given within one week of the initial date of exam.

COURSE OUTLINE

			Technical						
			PLO 1 (KW)			PLO2 (AP)		PLO 5 (CS)	
	No.	**Assessment**	**CLO1**	**CLO2**	**CLO3**	**CLO4**	**CLO 5**	**CLO 5**	**Total %**
	1	**LAB 1**				**3.5**			**3.5**
	2	**LAB 2**				**3.5**			**3.5**
	3	**LAB 3**				**3.5**			**3.5**
	4	**LAB 4**					**3.5**		**3.5**
	5	**PROJECT REPORT**						**5**	**6**
	6	**PROJECT DEMO**					**6**		**5**
	7	**TEST 1**	15						**15**
	8	**TEST 2**		**30**					**30**
	9	**FINAL EXAM**			**30**				**30**
	Total		15	32.35	27.65	10.5	8.5	6	**100**
			75			**20**		**5**	