Field of Computer Science
School of Computing, Faculty of Engineering
UNIVERSITI TEKNOLOGI MALAYSIA

COURSE : SECR1013 DIGITAL LOGIC

SESSION/SEM : 2021/2022 - 1

LAB 2 : COMBINATIONAL LOGIC CIRCUIT DESIGN SIMULATION USING DEEDS SIMULATOR

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A. Objective

i) To expose student with producing digital logic circuit, generating truth table with Deeds Simulator.

ii) To expose student with conversion between basic gates circuits and universal gates circuits.

iii) To expose student with a complete cycle process of a combinatorial circuit design and simulate with Deeds Simulator.

B. Material

Deeds Software for Windows.

Lab Activities

Part A

Simulating and converting logic circuit and construct truth table with Deeds.

1. Draw circuit in Figure 1 in Deeds.

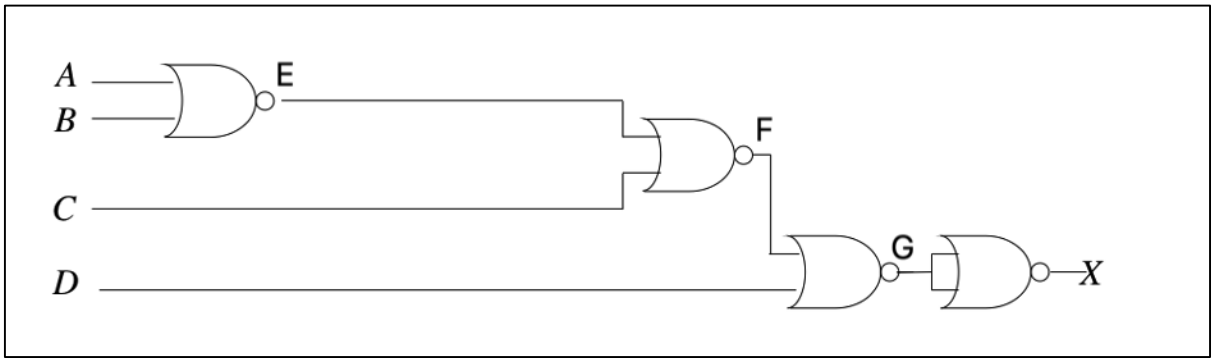


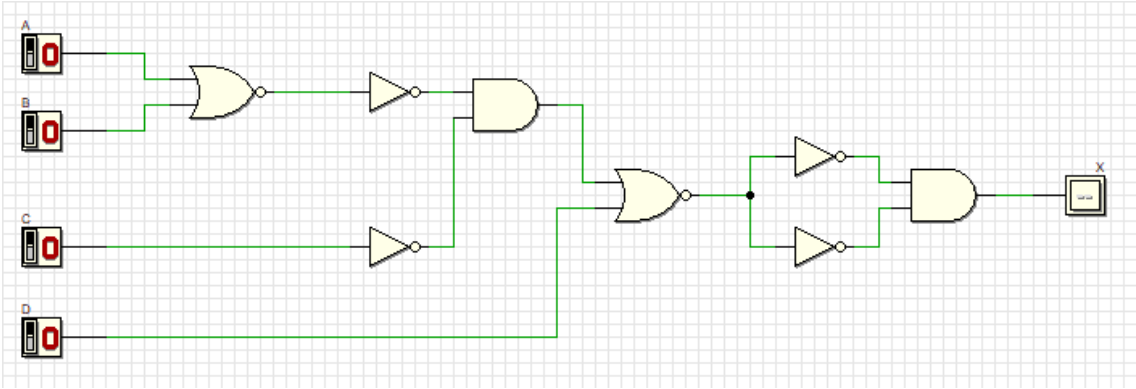
Figure 1: NOR Universal gates circuit

2. Simulate the circuit and built the truth table using the following headers.

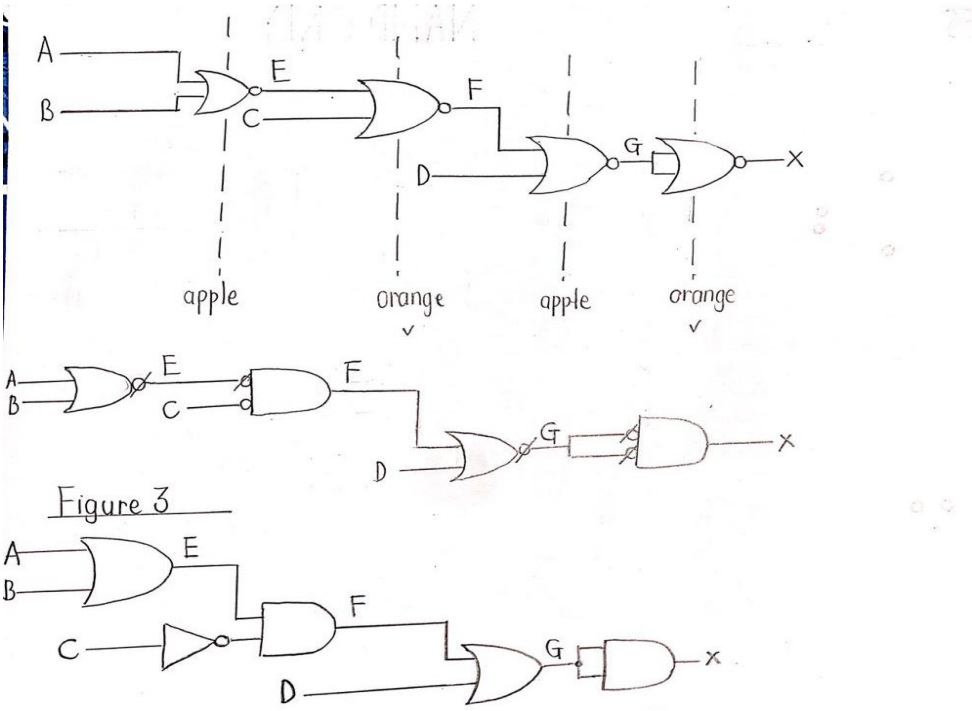
Truth Table 1

INPUT				OUTPUT			
A	**B**	**C**	**D**	**E**	**F**	**G**	**X**
0	0	0	0	1	0	1	0
0	0	0	1	1	0	0	1
0	0	1	0	1	0	1	0
0	0	1	1	1	0	0	1
0	1	0	0	0	1	0	1
0	1	0	1	0	1	0	1
0	1	1	0	0	0	1	0
0	1	1	1	0	0	0	1
1	0	0	0	0	1	0	1
1	0	0	1	0	1	0	1
1	0	1	0	0	0	1	0
1	0	1	1	0	0	0	1
1	1	0	0	0	1	0	1
1	1	0	1	0	1	0	1
1	1	1	0	0	0	1	0
1	1	1	1	0	0	0	1

3. Change the gates in your chosen level to dual symbol. Draw them using AND gate and 2 NOT gates in Deeds. Paste the circuit (Figure 2) here.



4. Simplified the circuit in Question 3. Paste the circuit (Figure 3) here.

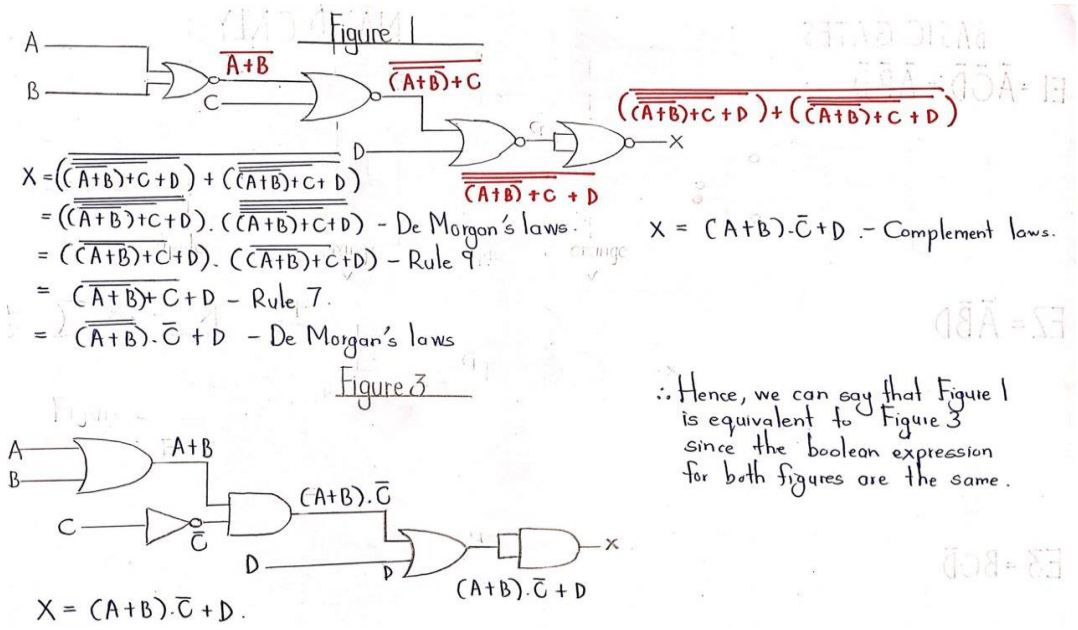


5. Confirm circuit in Figure 3 is equivalent to circuit in Figure 1 by simulating the circuit and building Truth Table 2.

INPUT				OUTPUT			
A	**B**	**C**	**D**	**E**	**F**	**G**	**X**
0	0	0	0	1	0	0	0
0	0	0	1	0	0	1	1
0	0	1	0	0	0	0	0
0	0	1	1	0	0	1	1
0	1	0	0	1	1	1	1
0	1	0	1	1	1	1	1
0	1	1	0	1	0	0	0
0	1	1	1	1	0	1	1
1	0	0	0	1	1	1	1
1	0	0	1	1	1	1	1
1	0	1	0	1	0	0	0
1	0	1	1	1	0	1	1
1	1	0	0	1	1	1	1
1	1	0	1	1	1	1	1
1	1	1	0	1	0	0	0
1	1	1	1	1	0	1	1

Based on the Truth Table 1 and Truth Table 2, we can conclude that Figure 1 is equal to Figure 3 since the output X for Truth Table 2 and Truth Table 1 have the same values.

6. Derive the output expression from Figure 1 and show that it is equivalent to the expressions from Figure 3.



Part B

Combinational circuit design process and simulate with Deeds Simulator.

Design Process

i) Determine Parameter Input/Output and their relations.
ii) Construct Truth Table.
iii) Using K-Map, get the SOP optimized form of all Boolean equation outputs.
iv) Draw the circuit and use duality symbol.
v) Simulate the design using Deeds Simulator. Check the results according to Truth Table.

Problem Situation

A new digital fault diagnoses circuit is requested to be designed for analysing four bit 2's complement input binary number from sensors A, B, C, and D. Sensor A represents input MSB and sensor D represents input LSB. As shown in the following Figure 5, bit pattern analysis from input sensors A, B, C, and D will trigger four different output errors (active HIGH) of type E1, E2, E3, and E4.

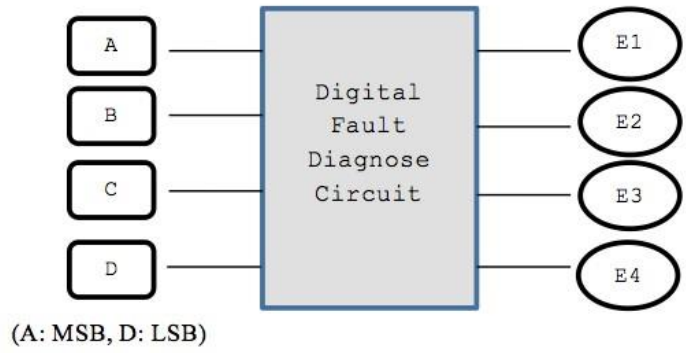


Figure 5

The following rules are used to activate the error's signal type:

RULE 1: E1 is activated if the input number is positive even and the majority of the bits is '0'.
RULE 2: E2 is activated if the input number is positive odd and the majority of the bits is '0'.
RULE 3: E3 is activated if the input number is negative even and the majority of the bits is '1'.
RULE 4: E4 is activated if the input number is negative odd and the majority of the bits is '1'.
RULE 5: The output of error signal is invalid if the input has equal bit '0' and bit '1'

NOTE: Positive odd is positive numbers that are odd
Negative even is negative numbers that are even.
Zero is considered positive number.

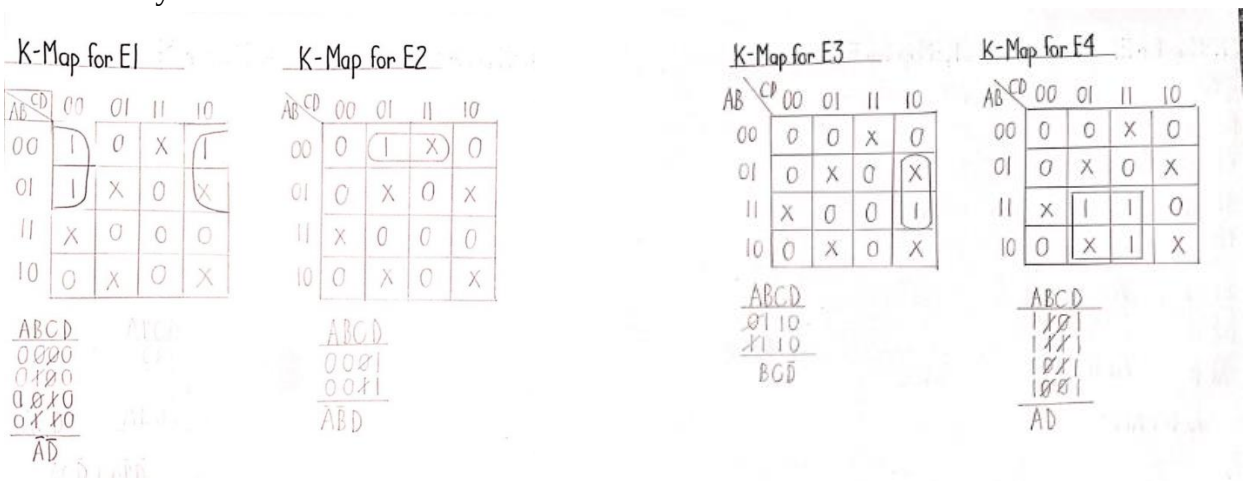
Experimental Steps

1. Create Truth Table 3 for Digital Fault Diagnose Circuit. Use variables A, B, C and D as inputs; E1, E2, E3 and E4 as outputs.

Truth Table 3

INPUT					OUTPUT			
DECIMAL	**A**	**B**	**C**	**D**	**E1**	**E2**	**E3**	**E4**
0	0	0	0	0	1	0	0	0
1	0	0	0	1	0	1	0	0
2	0	0	1	0	1	0	0	0
3	0	0	1	1	X	X	X	X
4	0	1	0	0	1	0	0	0
5	0	1	0	1	X	X	X	X
6	0	1	1	0	X	X	X	X
7	0	1	1	1	0	0	0	0
-8	1	0	0	0	0	0	0	0
-7	1	0	0	1	X	X	X	X
-6	1	0	1	0	X	X	X	X
-5	1	0	1	1	0	0	0	1
-4	1	1	0	0	X	X	X	X
-3	1	1	0	1	0	0	0	1
-2	1	1	1	0	0	0	1	0
-1	1	1	1	1	0	0	0	1

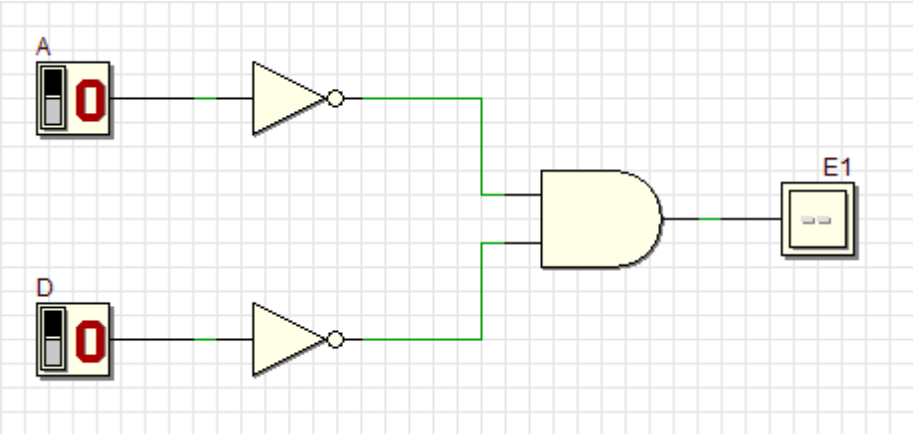
2. Using K-MAP, get minimized SOP Boolean expressions for E1, E2, E3 and E4 circuits. Paste your K-MAP here.



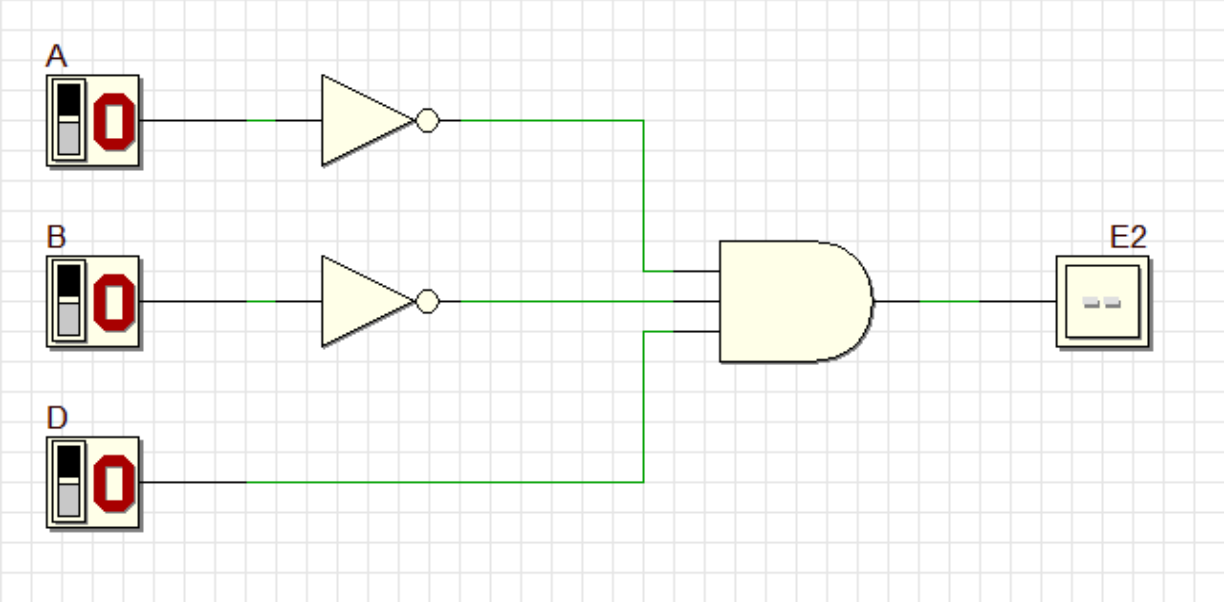
E1 = A'D'
E2 = A'B'D
E3 = BCD'
E4 = AD

3. From the Boolean expression in the step (2), draw your final E1, E2, E3 and E4 circuits. Use Deeds Simulator and paste your circuit here.

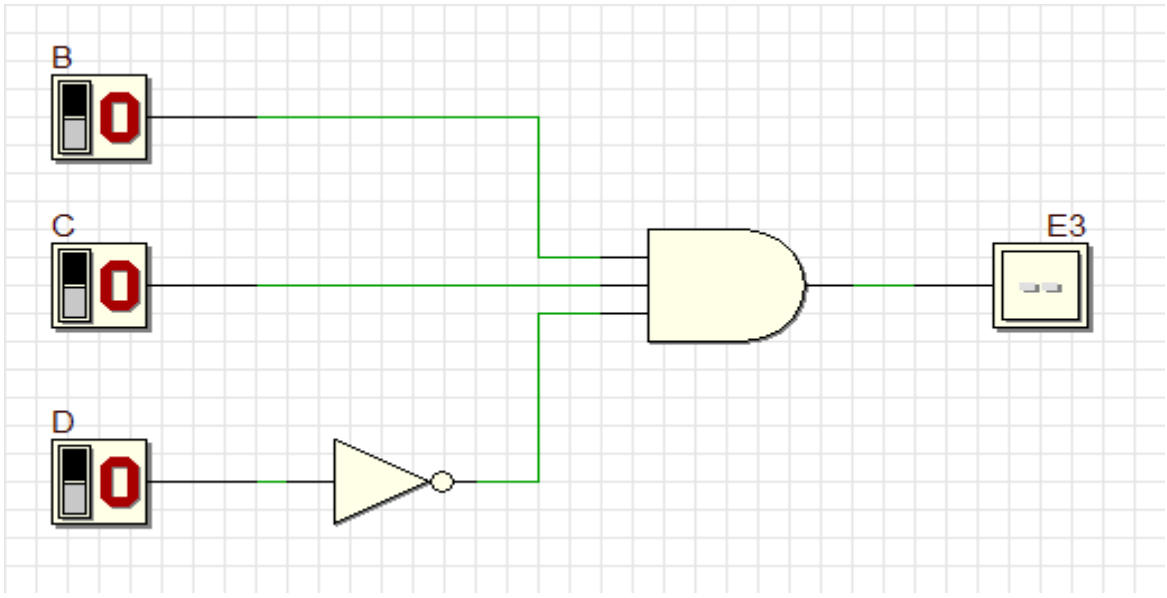
E1 = A'D'



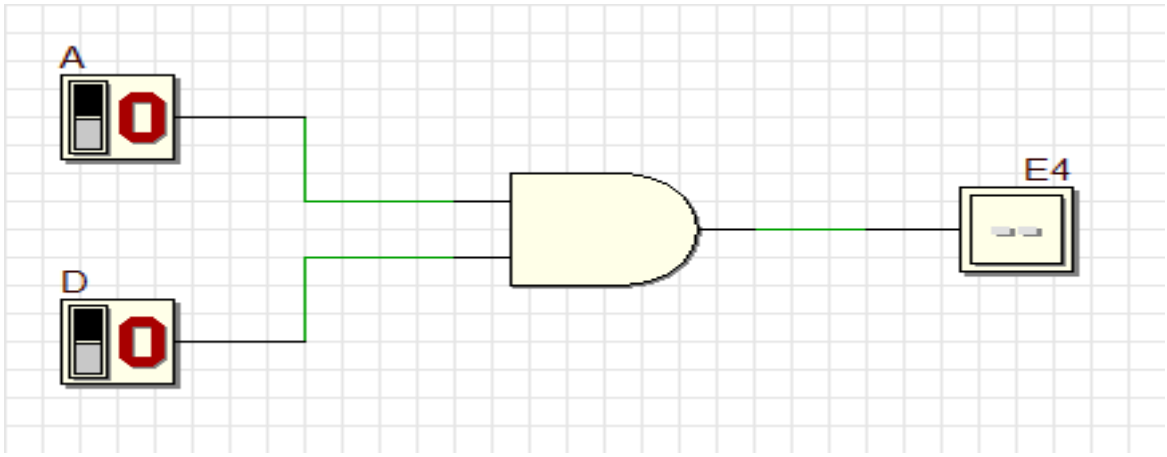
E2 = A'B'D



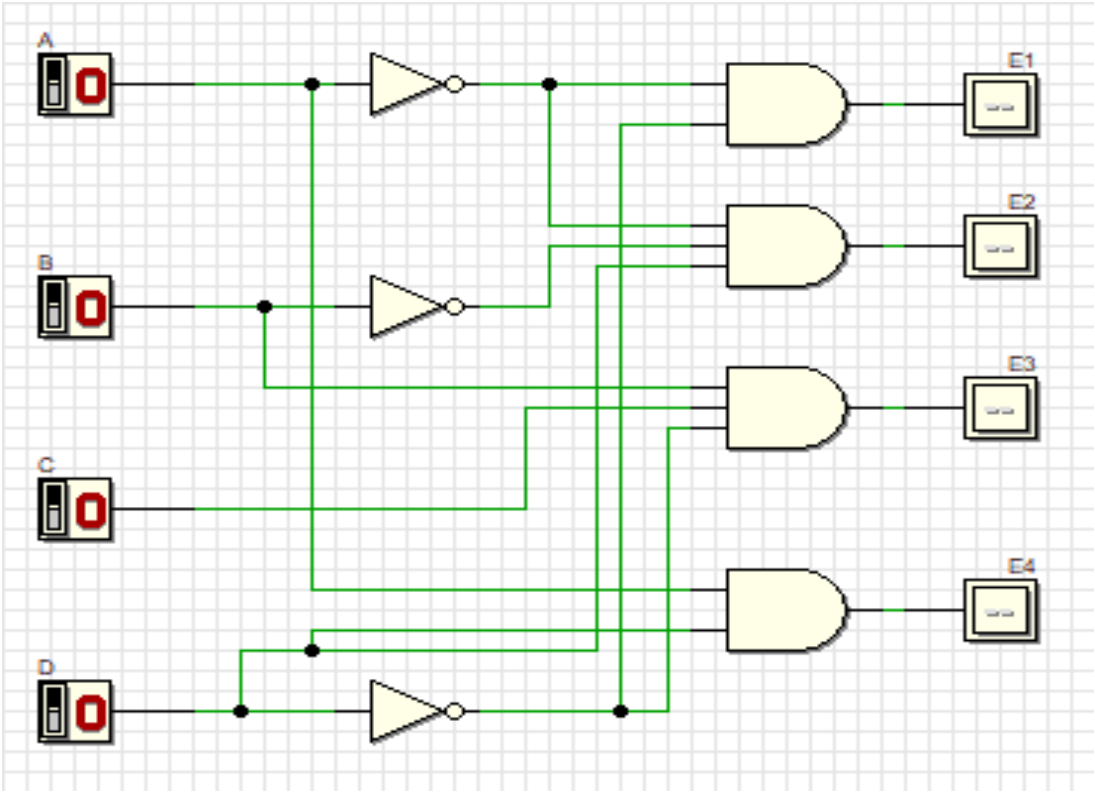
E3 = BCD’



E4 = AD



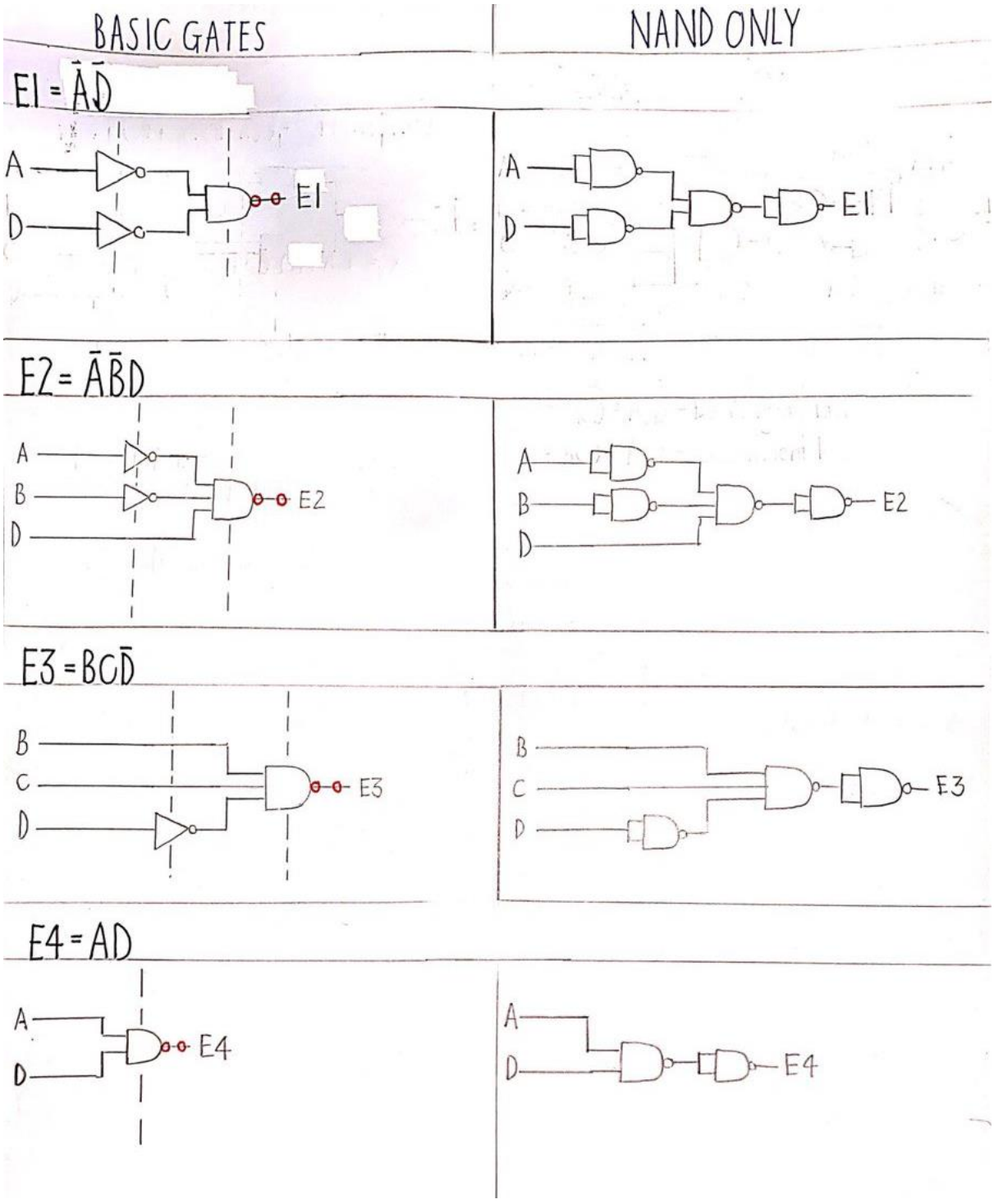
4. Simulate the Deeds circuit in step (3) and update Truth Table 4 based on the simulation result.



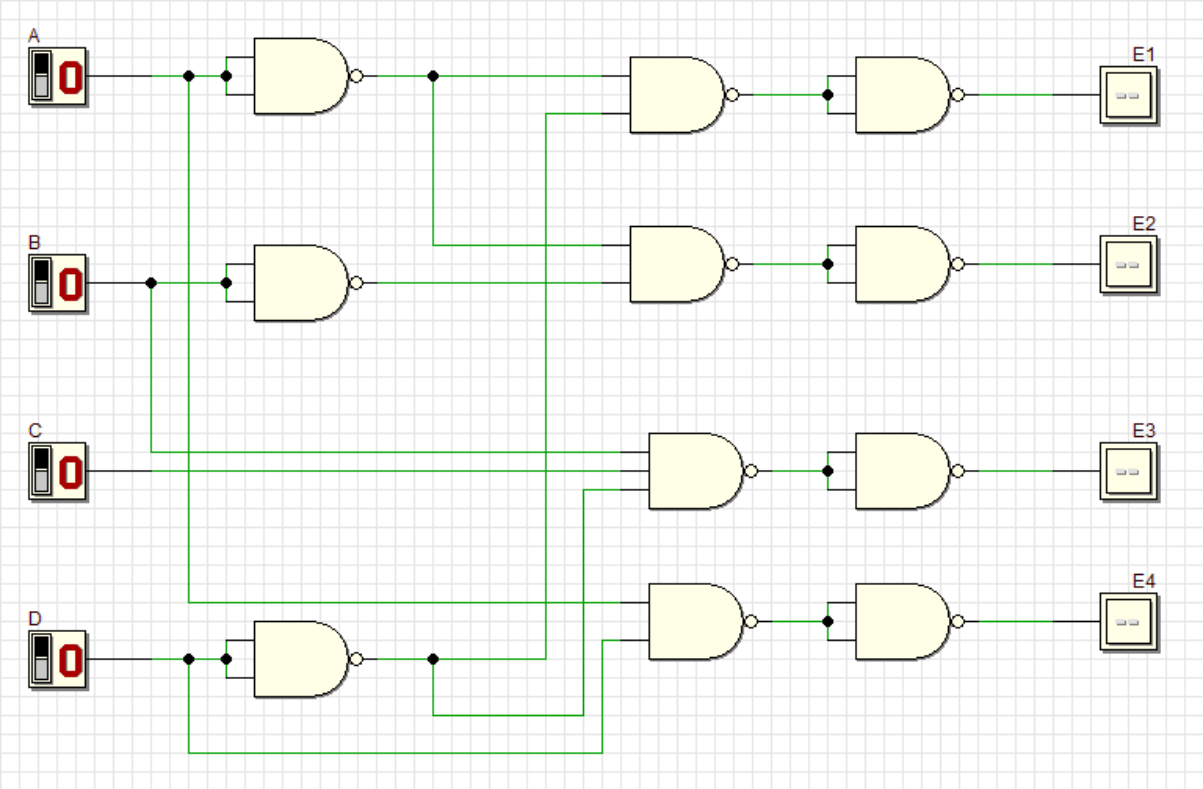
Truth Table 4

INPUT					OUTPUT			
DECIMAL	**A**	**B**	**C**	**D**	**E1**	**E2**	**E3**	**E4**
0	0	0	0	0	1	0	0	0
1	0	0	0	1	0	1	0	0
2	0	0	1	0	1	0	0	0
3	0	0	1	1	X	X	X	X
4	0	1	0	0	1	0	0	0
5	0	1	0	1	X	X	X	X
6	0	1	1	0	X	X	X	X
7	0	1	1	1	0	0	0	0
-8	1	0	0	0	0	0	0	0
-7	1	0	0	1	X	X	X	X
-6	1	0	1	0	X	X	X	X
-5	1	0	1	1	0	0	0	1
-4	1	1	0	0	X	X	X	X
-3	1	1	0	1	0	0	0	1
-2	1	1	1	0	0	0	1	0
-1	1	1	1	1	0	0	0	1

5. From the circuit in step (3), show the conversion of basic gates in E1, E2, E3 and E4 circuits to NAND universal gates. Post your workings here.



6. Draw the results of Step (5) in DEEDS. Post the circuits here.



7. Confirm your circuit by simulating the circuits. Make sure that the outputs are the same as Truth Table 3 and Truth Table 4.

Based on the Truth Table 3 and Truth Table 4, both circuits are equivalent since the outputs for Truth Table 3 and the outputs for the Truth Table 4 have the same values.

Edited by Marina Md Arshad, 28112021