COURSE OUTLINE

School / Faculty:	Computing / Engineering	**Page:**	1 of 5
Program Name:	BACHELOR OF COMPUTER SCIENCE (COMPUTER NETWORK & SECURITY)		
Course code:	SECR2033	**Academic Session/Semester:**	2020/2021-II
Course name:	COMPUTER ORGANIZATION AND ARCHITECTURE	**Pre/co requisite (course name and code, if applicable):**	SECR1013 DIGITAL LOGIC
Credit hours:	3		

Course synopsis	This course was designed to give the understanding of basic concept of computer organization and architecture. Topics covered in this subject will be on computer performance, types of data and the representative, arithmetic manipulation, instruction execution, micro programmable control memory, pipelining, memory, input/output and instruction format. At the end of this course, the student should be able to understand the concept of overall computer component and realize the current technology in computer hardware.
Course coordinator (if applicable)	

Course lecturer(s)/ Section	**Name**	**Office**	**E-mail**
01, 07	Dr Zuriahati Bt .Mohd Yunos	N28-438-02	zuriahati@utm.my
02, 08	Dr Aida Bt. Ali	N28-207-15	aida@utm.my
03	Dr Mohd Fo'ad B. Rohani	N28-347-02	foad@utm.my
04	PM Dr Mohd Murtadha B. Mohamad		murtadha@utm.my
05, 06, 10	Muhalim B. Mohamed Amin (P)	N28-346-05	muhalim@fc.utm.my
09	Dr Nur Haliza B. Abdul Wahab	N28A-02-11-01	nur.haliza@utm.my
15	Dr Muhammad 'Arif B. Mohamad	MJIIT-KL	muhammad.arif.kl@utm.my

Mapping of the Course Learning Outcomes (CLO) to the Programme Learning Outcomes (PLO), Teaching & Learning (T&L) methods and Assessment methods:

No.	**CLO**	**PLO (CODE)**	**Weight (%)**	***Taxonomies and **generic skills**	**T&L methods**	**Assessment methods*** **
CLO1	Describe the computer systems components and apply basic computer arithmetic.	PLO1 (KW)	10	C3, A2	Lecture, Active learning	T1
CLO2	Differentiate the different types of addressing modes and micro- instructions employed in a computer system.	PLO1 (KW)	10	C4, A2	Lecture, Active learning	T2
CLO3	Distinguish the different components of the computer systems (Control Unit, CPU, Memory and I/O) and measure their performances.	PLO1 (KW)	45	C5, A2	Lecture, Active learning	T2, F
CLO4	Design and implement low level coding for operational computer systems.	PLO2 (AP)	20	C4, TH1	Lab-based learning	L
CLO5	Demonstrate project deliverables in a group based on predefined specifications.	PLO6 (SC) PLO7 (TW)	15	SC2, SC3, TW1, TW4	Project-based learning	PR
Refer *Taxonomies of Learning and **UTM's Graduate Attributes, where applicable for measurement of outcomes achievement ***T – Test; L – Lab; PR – Project; Pr – Presentation; F – Final Exam etc.						

Prepared by: Name: Marina Bt. Md Arshad (Course Owner) Signature: Date: 6 Sept 2020	Certified by: Name: Prof. Dr. Md Asri B. Ngadi (Director of Computer Science) Signature: Date:

COURSE OUTLINE

School / Faculty:	Computing / Engineering	**Page:**	2 of 5
Program Name:	BACHELOR OF COMPUTER SCIENCE (COMPUTER NETWORK & SECURITY)		
Course code:	SECR2033	**Academic Session/Semester:**	2020/2021-II
Course name:	COMPUTER ORGANIZATION AND ARCHITECTURE	**Pre/co requisite (course name and code, if applicable):**	SECR1013 DIGITAL LOGIC
Credit hours:	3		

Details on Innovative T&L practices:

No.	Type	Implementation
1.	Active learning	Conducted through in-class activities.
2.	Project-based learning	Conducted through programming assignment. Students in a group of 3 are given 1 project that require assembly language solutions involving the problem specification and low-level machine coding using MS Visual Studio. Compliance to the problem specification need to be given in the form of written reports and source code.

Weekly Schedule:

Week	Topic	Activities
1 (14 Mac)	**MODULE 1: Basic Concepts and Computer Evolution** Course Overview, Main Components of Computer, Computer Structure and Functions, Computer Evolution, Computer Level Hierarchy	
2 (21 Mac) *	**MODULE 2: Data Representation in Computer Systems** Fixed-Number Representation, Fixed-Number Arithmetic Operations (Addition, Subtraction, Multiplication and Division), …	
3 (28 Mac)	… Floating-Number Representation (IEEE 754), Floating-Point Arithmetic (Addition and Multiplication).	☐ *Lab 1 (mov, add, sub)*
4 (4 Apr)	**MODULE 3: Introduction to Assembly Language Programming** Constant, Identifiers, Expression, Data Type, Little Endian, Basic Instructions	
5 (11 Apr) *	**MODULE 4: Instruction Set Architecture (ISA)** ISA Level, Element of Instructions, Instruction Types, Number of Addresses, …	☐ *Lab 2 (xchg, dec, inc, neg)*
6 (18 Apr)	… Registers, Type of Operands, Addressing Modes, Instruction Format	☐ *Test 1 (Module 1, 2) (20 Apr 2021)*
7 (25 Apr)	**MODULE 5: Central Processing Unit (CPU)** Datapath and Control Unit, Bus, Registers, Instruction Cycle (Fetch, Indirect, Execution, Interrupt)	☐ *Lab 3 (flags, offset, arrays, jmp, loop)*
8 (2 May)	Pipeline, Analogy Pipeline, Degree of Speedup, Instruction Pipeline, Pipeline Limitations, Resource Conflict, Data Dependency, Branch Difficulties	☐ *Lab 4 (conditional processing, Boolean instructions)*
9 (9 May) *	MID-SEMESTER BREAK	

COURSE OUTLINE

10 (16 May)	Control Unit (CU) Operation, Micro-operations, CU Functions, Microinstruction, Micro-programmed CU, Control Memory.	
11 (23 May) *	**MODULE 6: Memory System** Memory Hierarchy, Random Access, Direct Access and Sequential Access, Main Memory - Types; RAM and ROM, Memory Location and Capacity, Latency and Cycle Time, Transfer Rate and Bandwidth, Memory Interleaving; HOI and LOI	☐ *Test 2 (Module 3, 4) (18 May 2021)*
12 (30 May) *	Cache Memory: Cache Memory Principle, Cache Address Mapping Schemes - Direct Mapping, Block Direct Mapping, Fully Associative Mapping, Set Associative Mapping, Replacement Policy, Write Policy, Average Memory Access Time, Multilevel Caches, Virtual Memory	☐ *Lab 5 (input / output library functions)*
13 (6 Jun)	**MODULE 7: Input / Output (I/O) and Storage System** I/O and Performance, I/O Architectures - Programmed I/O, Interrupt Driven I/O, Direct Memory Access (DMA), Channel I/O, Storage Systems, Magnetic Disk Technology, Optical Disks, Magnetic Tape, RAID	☐ *Lab 6 (conditional structures)*
14 (13 Jun)	**MODULE 8: Performance Measurements and Analysis** Computer Performance Measures and Equation, CPU Execution Time, CPI, Increasing CPU Performance, Comparing CPU Performance, Average System Performance, Comparing Relative Performance, Benchmarking	☐
16 (27 Jun)	**Study Week**	

* *Public Holidays:*

Birthday of His Majesty the Sultan of Johor (23 Mac); 1st of Ramadan (13 Apr); Eid Al-Fitri (13-14 May); Wesak Day (26 May); Gawai Dayak (1 Jun);

Transferable skills (generic skills learned in course of study which can be useful and utilised in other settings):

Team working, Scholarship

Student Learning Time (SLT) details:

L: Lecture, P: Practical (Lab), O: Others

Distribution of course content	Teaching and Learning Activities						TOTAL SLT
	Guided Learning (Face to Face)				Guided Learning Non-Face to Face	Independent Learning Non-Face to face	
CLO	**L**	**T**	**P**	**O**			
CLO 1	6	2	1			9.75	**16h 45m**
CLO 2	8	2	2			10	**20h**
CLO 3	14	3	3			16	**34h**
CLO 4			12		1	7	**20h**

COURSE OUTLINE

Program Name:	BACHELOR OF COMPUTER SCIENCE (COMPUTER NETWORK & SECURITY)		
Course code:	SECR2033	**Academic Session/Semester:**	2020/2021-II
Course name:	COMPUTER ORGANIZATION AND ARCHITECTURE	**Pre/co requisite (course name and code, if applicable):**	SECR1013 DIGITAL LOGIC
Credit hours:	3		

CLO 5				1	1	10	**12h**
Total SLT	**28h**	**7h**	**18h**	**1h**	**2h**	**52h 45m**	**113h 45m**

Continuous Assessment		PLO	Percentage	Total SLT
1	Lab 1 - 6	PLO2 (AP)	20	**As in CLO4**
2	Test 1	PLO1 (KW)	10	**1h 15m**
3	Test 2	PLO1 (KW)	20	**2h**
4	Group Project	PLO8 (SC), PLO7 (KW)	15	**As is CLO5**
Final Assessment			Percentage	Total SLT
1	Final Examination	PLO1 (KW)	35	**2.5**
Grand Total SLT			**100**	**120h**

Special requirement to deliver the course (*e.g*: software, nursery, computer lab, simulation room):

Computer lab with MS Visual Studio 2010

Learning resources:

Text book

W. Stalling, Computer Organization and Architecture, 10th Edition, Prentice Hall, 2016. RM82

Main references

L. Null & J. Lobur, The Essentials of Computer Organization and Architecture, 4th Edition, 2015. Kip R. Irvine, Assembly Language for Intel-based Computers, Prentice Hall, 6th edition, 2011.

Additional references

David Patterson and John Hennessy, Computer Organization and Design: The Hardware/Software Interface, 5th Edition, Morgan Kaufmann, 2014.

Mano, M. Morris, Computer System Architecture, 3rd Edition, Prentice-Hall, 1993.

Online

http://elearning.utm.my

COURSE OUTLINE

School / Faculty:	Computing / Engineering	**Page:**	5 of 5
Program Name:	BACHELOR OF COMPUTER SCIENCE (COMPUTER NETWORK & SECURITY)		
Course code:	SECR2033	**Academic Session/Semester:**	2020/2021-II
Course name:	COMPUTER ORGANIZATION AND ARCHITECTURE	**Pre/co requisite (course name and code, if applicable):**	SECR1013 DIGITAL LOGIC
Credit hours:	3		

Academic honesty and plagiarism:

Assignments are individual tasks and NOT group activities (UNLESS EXPLICITLY INDICATED AS GROUP ACTIVITIES). Copying of work (texts, lab results etc.) from other students/groups or from other sources is not allowed. Brief quotations are allowed and then only if indicated as such. Existing texts should be reformulated with your own words used to explain what you have read. It is not acceptable to retype existing texts and just acknowledge the source as a reference. Be warned: students who submit copied work will obtain a mark of **zero** for the assignment and exams and disciplinary steps may be taken by the Faculty. It is also unacceptable to do somebody else's work, to lend your work to them or to make your work available to them to copy.

Other additional information (Course policy, any specific instruction etc.):

1. Attendance is compulsory and will be taken in every lecture session. Student with less than 80% of total attendance is not allowed to sit for final exam.
2. Students are required to behave and follow the University's dressing regulation and etiquette all the time.
3. Exercises and tutorial will be given in class and some may be taken for assessment. Students who do not do the exercise will lose the coursework marks for the exercise.
4. Assignments must be submitted on the due dates. Some points will be deducted for late submissions. Assignments submitted three days after the due date will not be accepted.
5. Make up exam will not be given, except to students who are sick and submit medical certificate confirmed by UTM panel doctors. Make up exam can only be given within one week of the initial date of exam.

No	Assessment	PLO1 (KW)			PLO2 (AP)	PLO6 (SC)	PLO7 (TW)	TOTAL
		CLO1	CLO2	CLO3	CLO4	CLO5	CLO5	
1	LABS (6)				20			20
2	TEST 1	10						10
3	TEST 2		10	10				20
4	FINAL EXAM			35				35
5	PROJECT REPORT					10	5	15
TOTAL PLO		65			20	10	5	100

Disclaimer: