D. Lab Activities

Part 1

Simulating logic circuit, construct truth table and timing diagram with Deeds.

Given Boolean expression as follow:

$$Y = AB + BC + AC$$

1. Convert the non-standard Boolean expression into standard form.

$Y = AB(C + \bar{C}) + (A + \bar{A})BC + A(B + \bar{B})C$

$= ABC + AB\bar{C} + ABC + \bar{A}BC + ABC + A\bar{B}C$

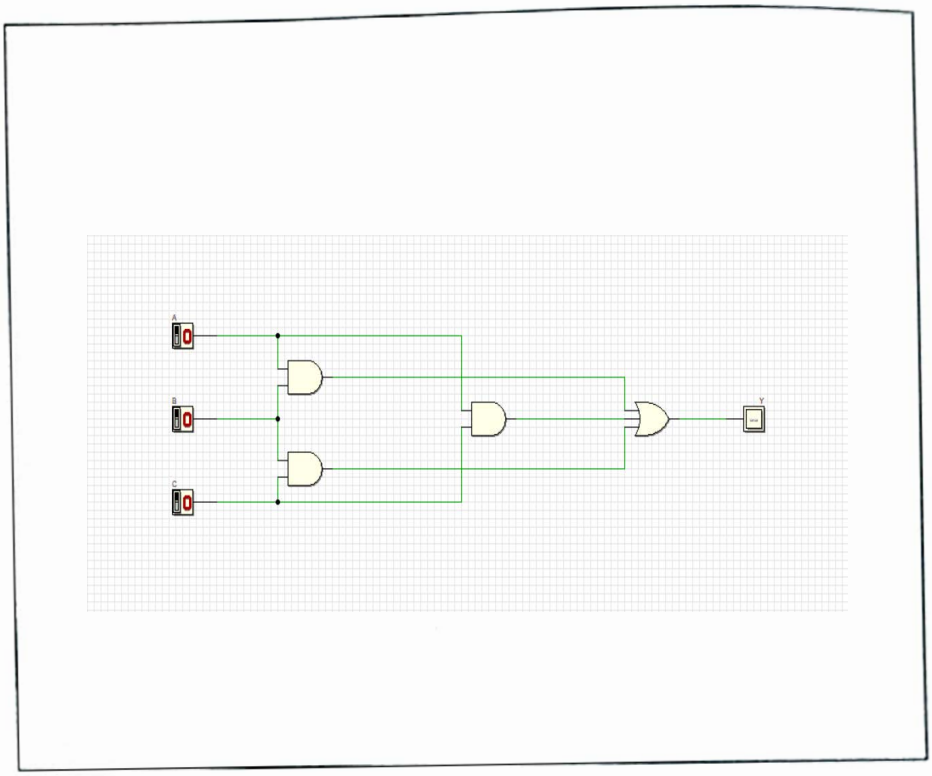
$= ABC + \bar{A}BC + A\bar{B}C + AB\bar{C}$

2. Based on standard form expression, complete the following truth table.

INPUT			OUTPUT
A	B	C	Y
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

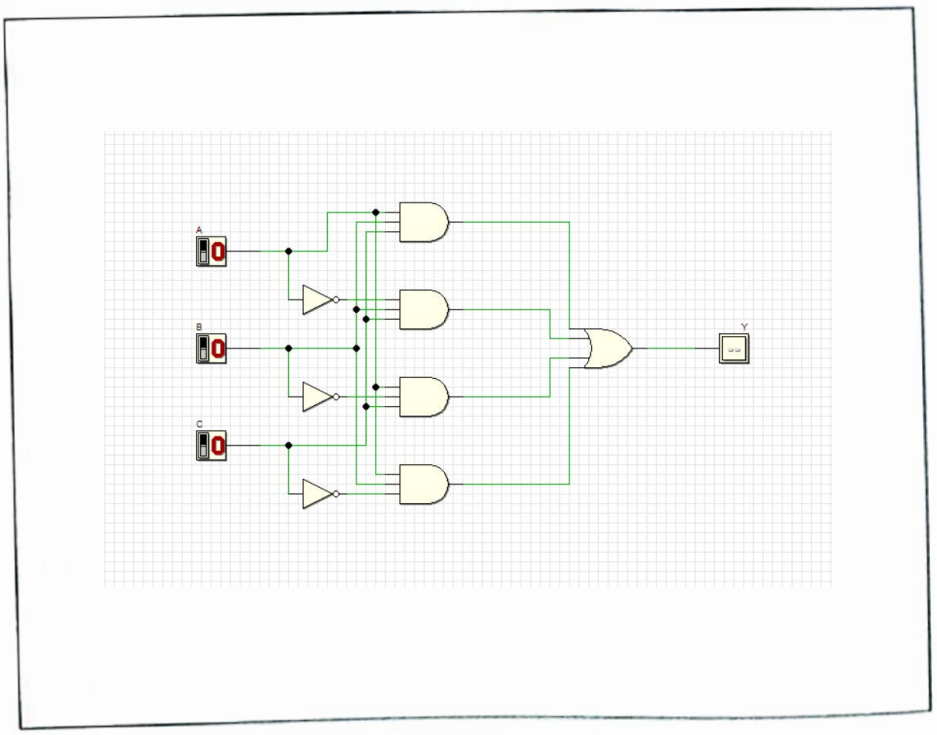
3. Using Deeds Simulator, draw the following circuits:

a) Circuit (i) for non-standard form (based on the given expression).



Circuit (i)

b) Circuit (ii) for standard form (from your answer in question (1)).



Circuit (ii)

4. Simulate these two circuits in step (3) and complete their truth table.

Compare the simulation result for these two truth tables. What is your conclusion?

Circuit (i)

INPUT			OUTPUT
A	B	C	Y
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

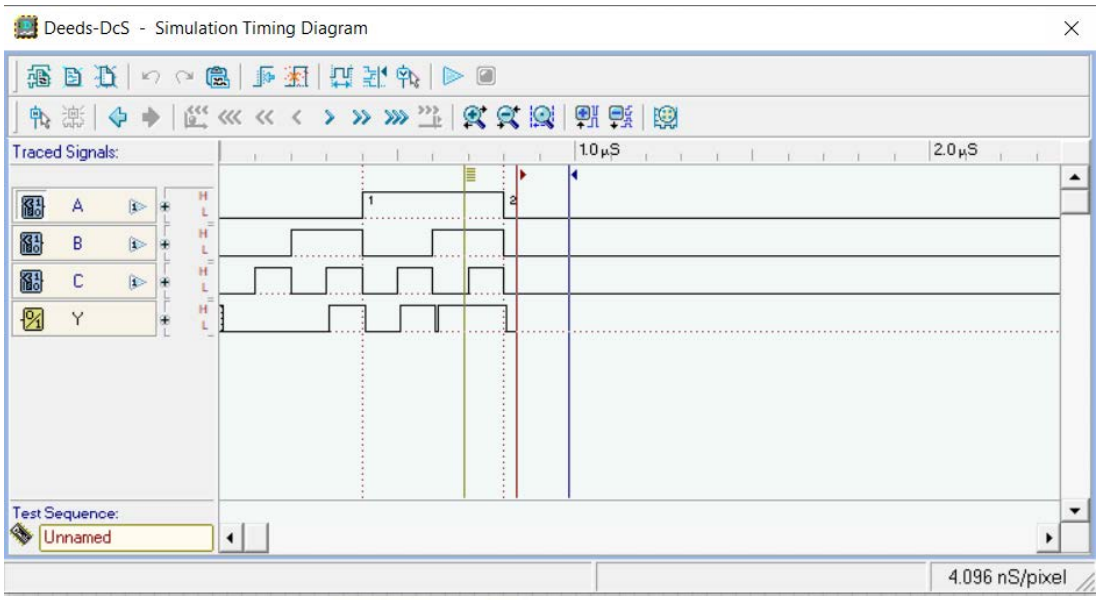
Circuit (ii)

INPUT			OUTPUT
A	B	C	Y
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

Conclusion:

Circuit (i) and Circuit (ii) are the same because they produce same output with same inputs.

5. Simulate output of circuit (ii) with Timing Diagram. Illustrate some examples of different inputs and output.



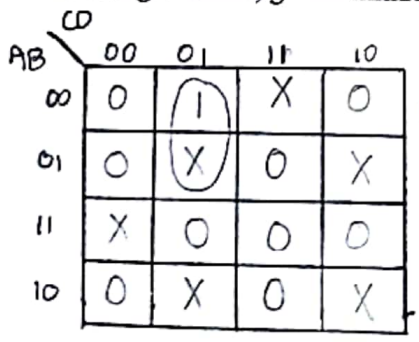
Experimental Steps

1. Complete Truth Table 1 for Digital Fault Diagnose Circuit. Use variables A, B, C and D as inputs; E1, E2, E3 and E4 as outputs.

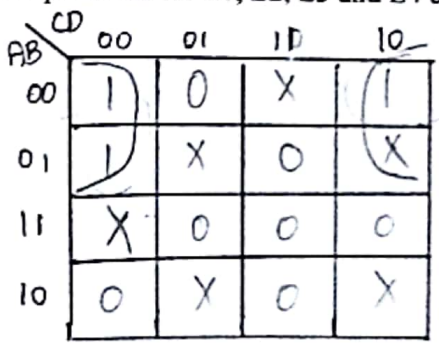
Truth Table 1

INPUTS				OUTPUTS			
A	B	C	D	E1	E2	E3	E4
0	0	0	0	0	1	0	0
0	0	0	1	1	0	0	0
0	0	1	0	0	1	0	0
0	0	1	1	X	X	X	X
0	1	0	0	0	1	0	0
0	1	0	1	X	X	X	X
0	1	1	0	X	X	X	X
0	1	1	1	0	0	0	0
1	0	0	0	0	0	0	0
1	0	0	1	X	X	X	X
1	0	1	0	X	X	X	X
1	0	1	1	0	0	1	0
1	1	0	0	X	X	X	X
1	1	0	1	0	0	1	0
1	1	1	0	0	0	0	1
1	1	1	1	0	0	1	0

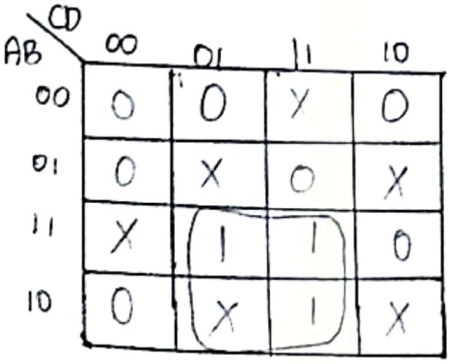
2. Using K-MAP, get minimized SOP Boolean expressions for E1, E2, E3 and E4 circuits.



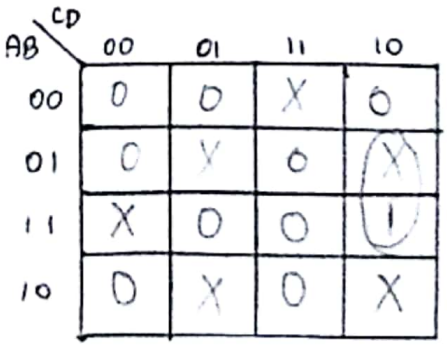
$E1 = \bar{A}\bar{C}D$



$E2 = \bar{A}\bar{D}$

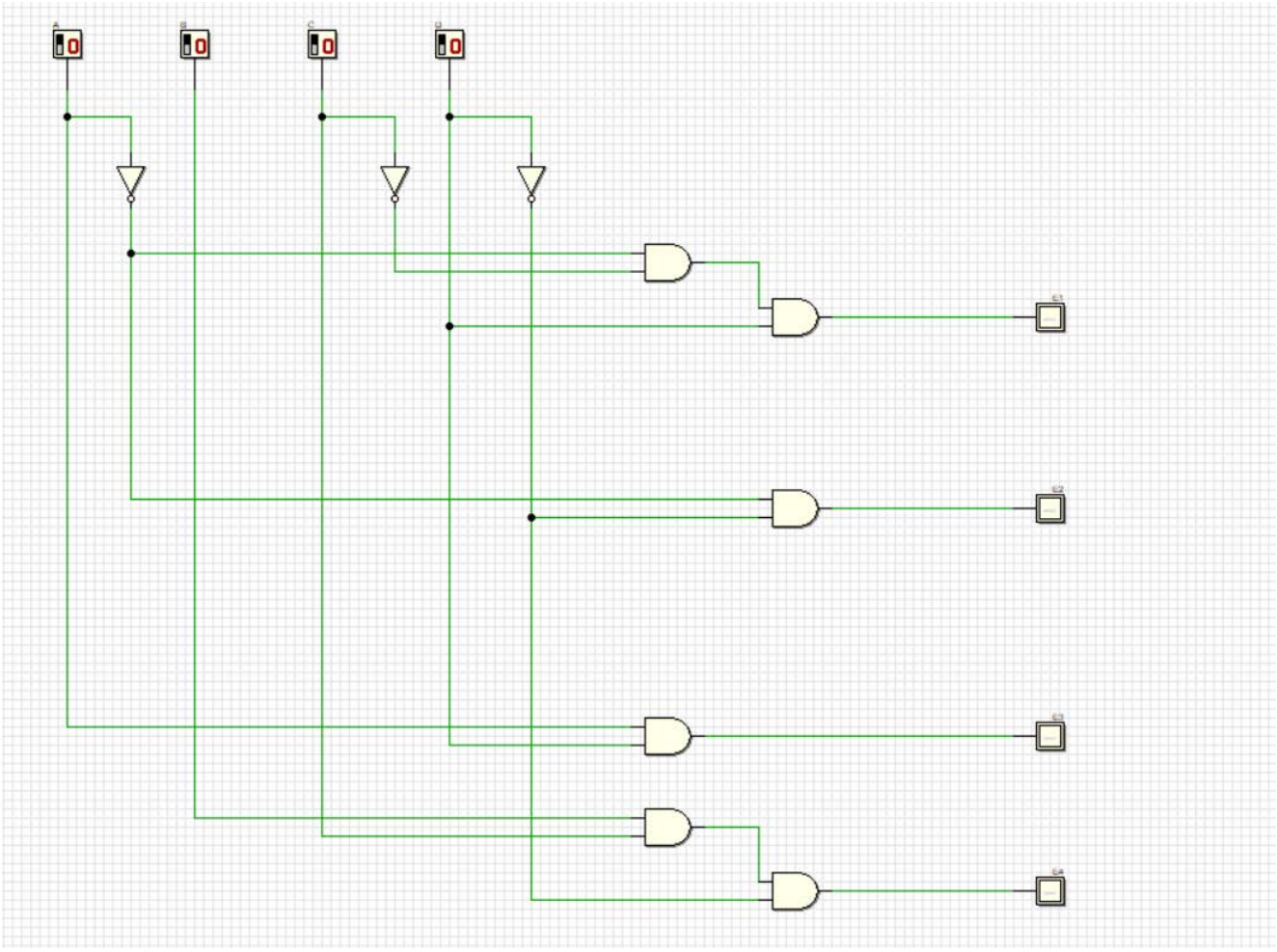


$E3 = AD$



$E4 = BC\bar{D}$

3. From the Boolean expression in the step (2), draw your final E1, E2, E3 and E4 circuits using 2 input basic gates (AND, OR, NOT). Use Deeds Simulator.



4. Simulate the Deeds circuit in step (3):

a) Update Truth Table 2 based on the simulation result.

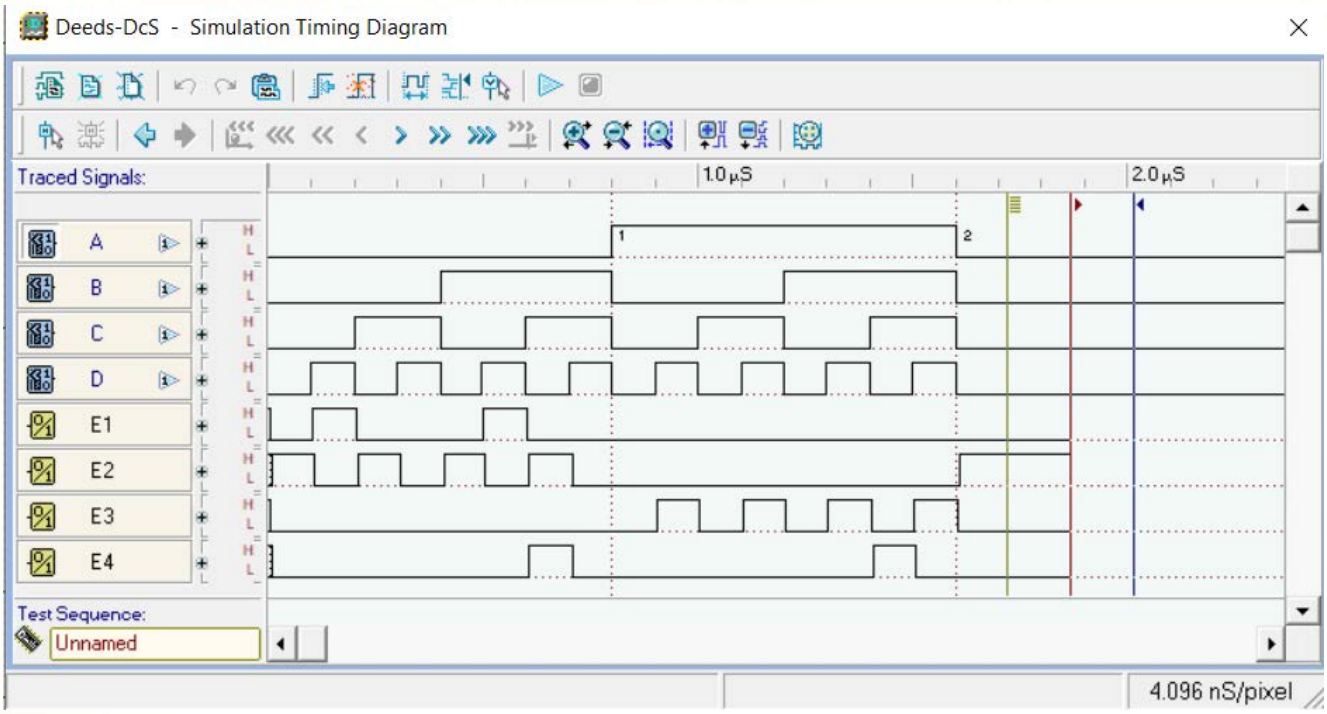
Truth Table 2

INPUTS				OUTPUTS			
A	B	C	D	E1	E2	E3	E4
0	0	0	0	0	1	0	0
0	0	0	1	1	0	0	0
0	0	1	0	0	1	0	0
0	0	1	1	0	0	0	0
0	1	0	0	0	1	0	0
0	1	0	1	1	0	0	0
0	1	1	0	0	1	0	1
0	1	1	1	0	0	0	0
1	0	0	0	0	0	0	0
1	0	0	1	0	0	1	0
1	0	1	0	0	0	0	0
1	0	1	1	0	0	1	0
1	1	0	0	0	0	0	0
1	1	0	1	0	0	1	0
1	1	1	0	0	0	0	1
1	1	1	1	0	0	1	0

Compare the output results in Truth Table 2 with Truth Table 1. What is your conclusion?

The output results in Truth Table 2 and Truth Table 1 are the same except for the invalid inputs. The output result of invalid inputs in Truth Table 1 is X while the output result of invalids inputs in Truth Table 2 is either '0' or '1'. The output results of valid inputs in Truth Table 2 and Truth Table 1 are the same. Therefore, the circuit in step(3) and Digital Fault Diagnose Circuit have same function when using valid inputs.

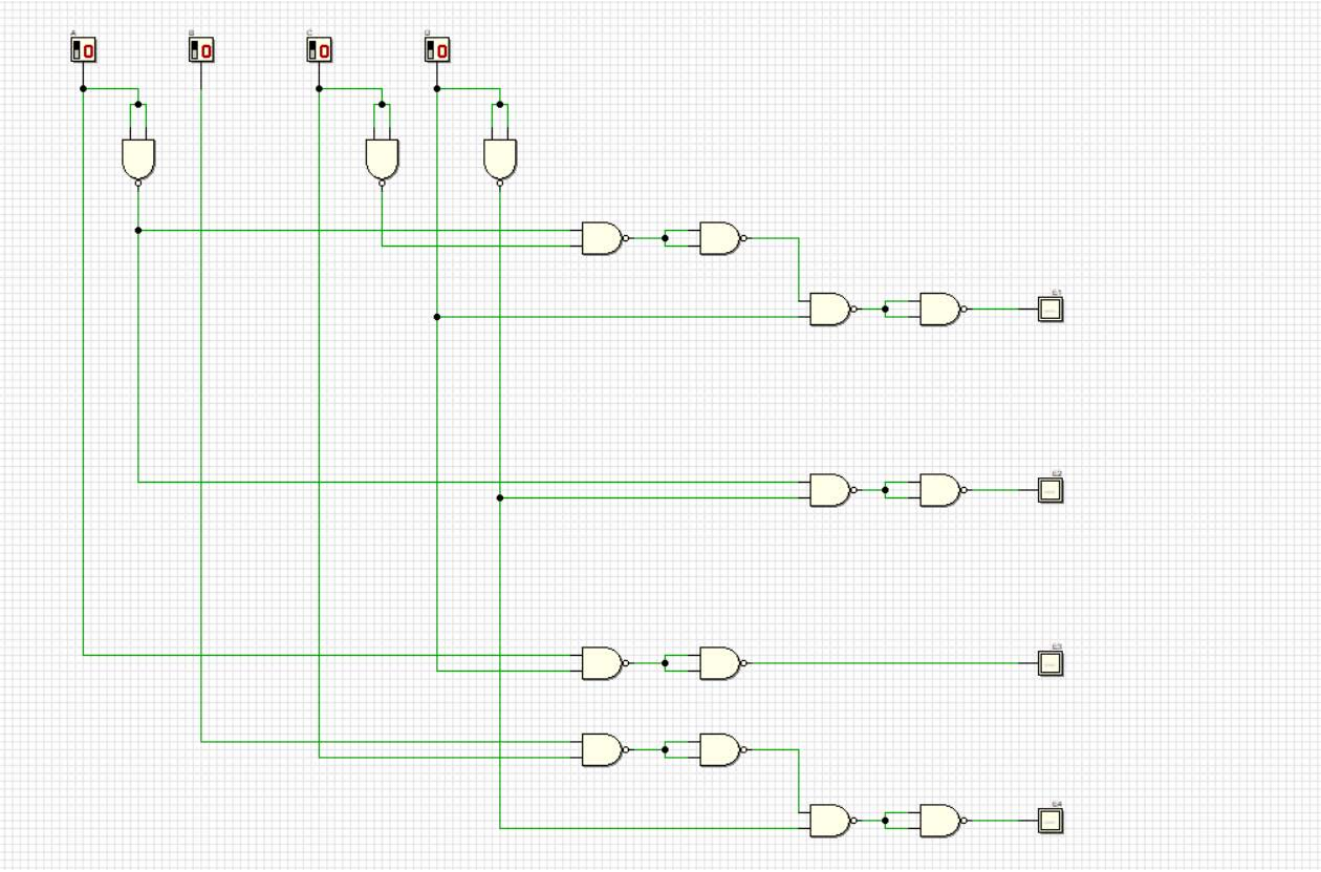
b) Timing Diagram



Explain some analysis values based on your timing diagram:

E1 has output '1' when the input A and input C are '0' and input D is '1'. E2 has output '1' when input A and D are '0'. E3 has output '1' when input A and D are '1'. E4 has output '1' when input B and C are '1' and input D is '0'. The result of timing diagram is same with the result of Truth Table 2.

5. Using dual symbol concept, convert your circuit in step (3) to NAND gates only. Use Deeds Simulator.



6. Simulate the Deeds circuit in step (5):

a) Update Truth Table 3 based on the simulation result.

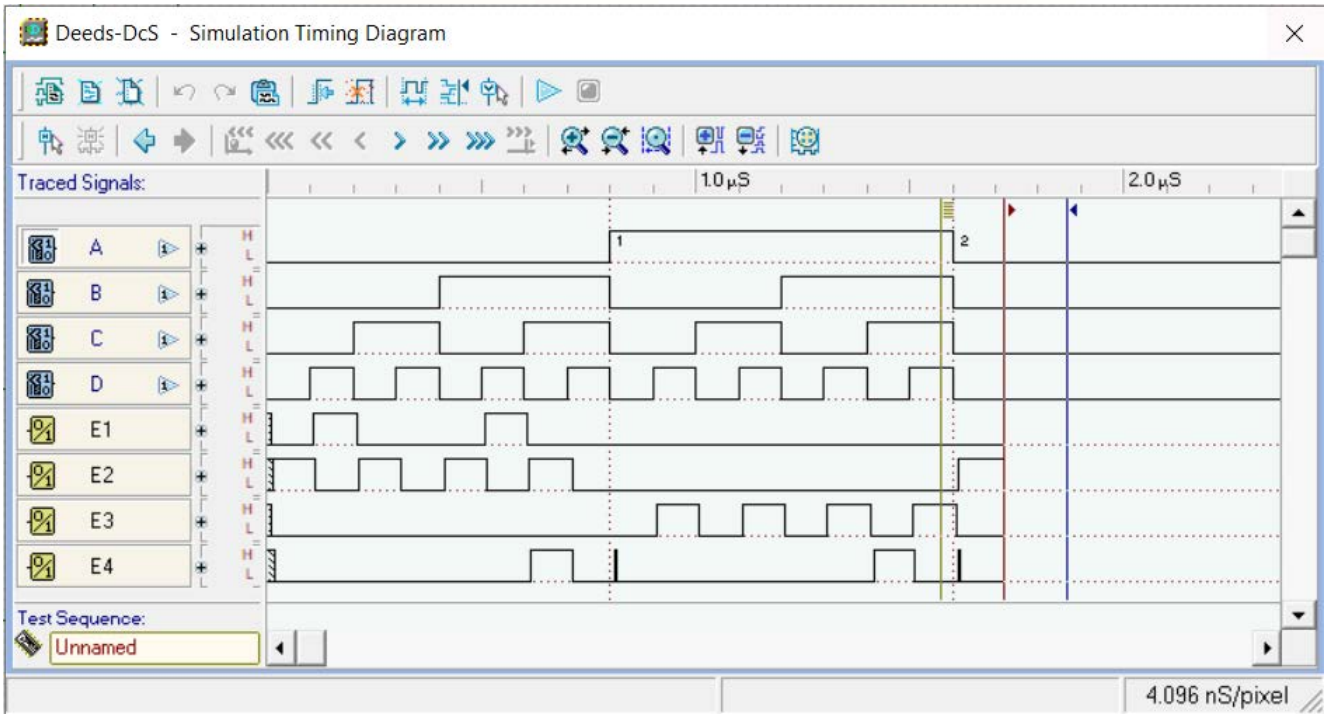
Truth Table 3

INPUTS				OUTPUTS			
A	B	C	D	E1	E2	E3	E4
0	0	0	0	0	1	0	0
0	0	0	1	1	0	0	0
0	0	1	0	0	1	0	0
0	0	1	1	0	0	0	0
0	1	0	0	0	1	0	0
0	1	0	1	1	0	0	0
0	1	1	0	0	1	0	1
0	1	1	1	0	0	0	0
1	0	0	0	0	0	0	0
1	0	0	1	0	0	1	0
1	0	1	0	0	0	0	0
1	0	1	1	0	0	1	0
1	1	0	0	0	0	0	0
1	1	0	1	0	0	1	0
1	1	1	0	0	0	0	1
1	1	1	1	0	0	1	0

Compare the output results in Truth Table 3 with Truth Table 2. What is your conclusion?

The output results in Truth Table 3 and Truth Table 2 are the same for all inputs. Therefore, circuit in step (5) and circuit in step (3) are the same.

b) Timing Diagram



Explain some analysis values based on your timing diagram:

E1 has output '1' when input A and C are '0' and input D is '1'. E2 has output '1' when input A and D are '0'. E3 has output '1' when input A and D are '1'. E4 has output '1' when input B and C are '1' and input D is '0'. The result of timing diagram is same with the result of Truth Table 3

Fully Completed ☐ Partially Completed ☐ Checked by: _____